

# **PRACTICAL POWER SOLUTIONS**



## **Acknowledgments:**

Thanks are due the many technical staff members of Analog Devices in Engineering, Marketing, and Applications who provided invaluable inputs during this project.

Special thanks go to Wayne Rewinkle, Matt Kessler, Brian Goeres, and Hank Zumbahlen who provided major contributions and also reviewed all the material.

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Analog Devices Central Applications Department

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**ISBN-13: 978-0-916550-00-4**

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## Practical Power Solutions

1. Point-of-Load Power
2. System Power Management and Portable Power
3. Power for Mixed Analog/Digital Systems
4. Hardware Design Techniques

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### SECTION 1 POINT-OF-LOAD POWER

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# Fixed Power Point-of-Load Applications

Today's system power requirements have become quite challenging, and design engineers must deal with multiple supply voltages, sequencing issues, high transient load currents, thermal considerations, and many others. In most cases, these problems must be addressed at the PC board level, and not at the system power supply. Therefore, some type of point-of-load (POL) power supplies are required on most PC boards, even those of modest complexity.

This seminar is aimed at design engineers who are not power supply experts, but must deal with the design of these POL supplies as part of their general system design projects.

In this section of the seminar we will discuss some important issues relating to powering non-portable systems, focusing primarily on digital system power (as opposed to analog power). Non-portable systems are often referred to as "fixed power" systems, and generally imply any system that does not operate on a battery. Specific issues relating to powering sensitive analog circuits can be found in Section 3 of the seminar.

This section also touches briefly on the fundamental concepts of linear and switching regulators, without delving into the detailed mathematical issues and theory relating to their design. Complete coverage of these topics can be found in textbooks as well as in online material. We believe that system design engineers are more interested in how comprehensive design tools can provide solutions to their specific power application problems.



## "Fixed Power" and "Portable Power" Applications

### **Fixed Power**

- ◆ **Does Not Require Battery (except for "keep alive" functions)**
- ◆ **Desktop Computers**
- ◆ **Base Stations**
- ◆ **Servers**



### **Portable Power**

- ◆ **Requires a Battery to Operate**
- ◆ **Notebook Computers**
- ◆ **Handsets**
- ◆ **Handheld Electronics**



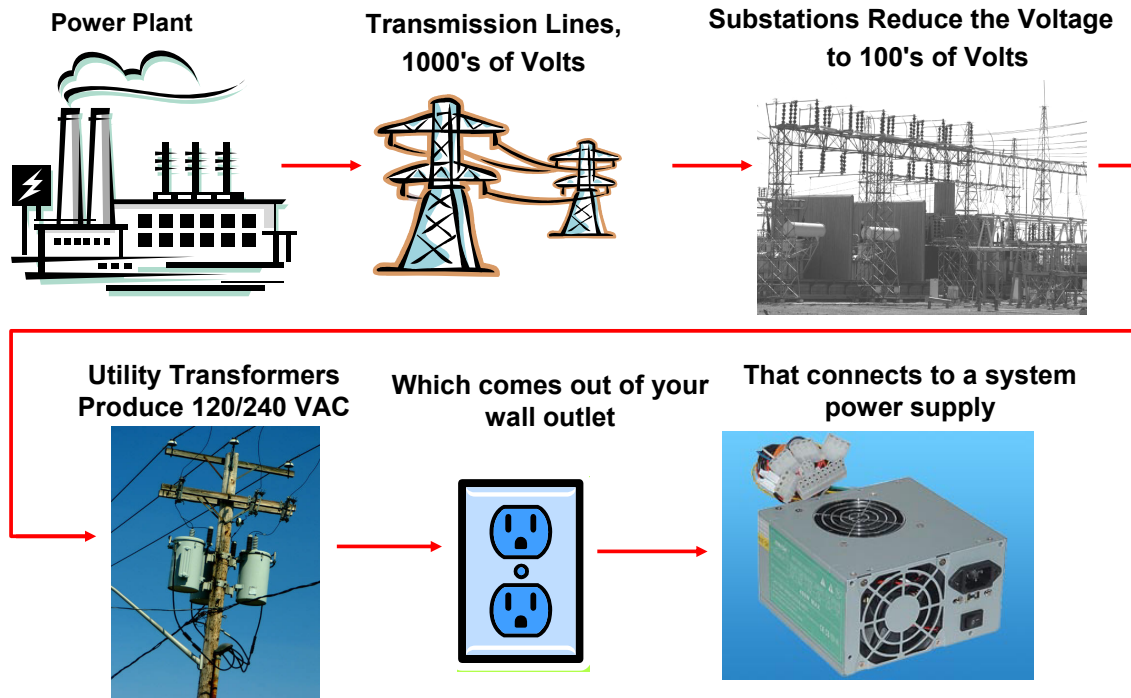
For the purposes of this seminar, system power applications are divided into two broad categories: fixed and portable.

"Fixed" power applications are those that do not require a battery (except for "keep alive" or memory backup functions).

Portable power applications require a battery for operation.

Although there is much commonality in powering the two types of systems, portable systems have certain specific requirements relating to efficiency, size, cost, and weight. The issues important to portable systems are covered in Section 2 of this seminar.

## Power Distribution System-1 (Down We Go in Voltage)



This figure illustrates how power is distributed from the power plant to the system power supply.

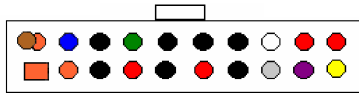
Power from the power plant is distributed to the substations over high voltage transmission lines at 1000's of volts. Since the product of the voltage,  $V$ , and the current,  $I$ , at any point in the system is constant ( $P = V \times I$ ), the use of high distribution voltages reduces the current flow through the lines and hence the  $I^2R$  losses. For a given amount of transmission line resistance, it is always more efficient to transmit power at voltages which are as high as practical.

The substations reduce the voltage to 100's of volts, and utility transformers reduce the voltage for home or business to 480 V, 240 V, or 110 V.

The same principle of power distribution is applicable to the system power supply as shown in the next figure.

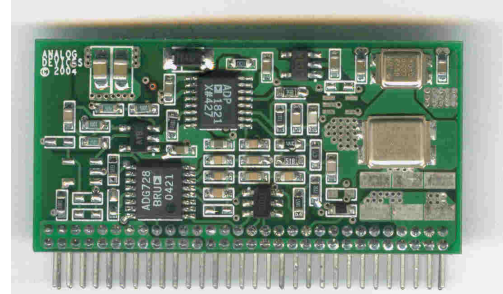
## Power Distribution System-2 (Down We Go in Voltage)

That provides some moderately low voltages at its output Connector



***3.3V, 5V, 12V***

Which powers a POL Power Converter that produces  $0.5V < V_{out} < 2.5V$



That powers the processor or other power-hungry device



A desktop computer power supply is a good example of a "fixed" power application. The power supply converts the ac line voltage to a number of common individual voltages which are distributed from the power supply to the various PC boards in the system. This figure shows common distribution voltages of 3.3 V, 5 V, and 12 V.

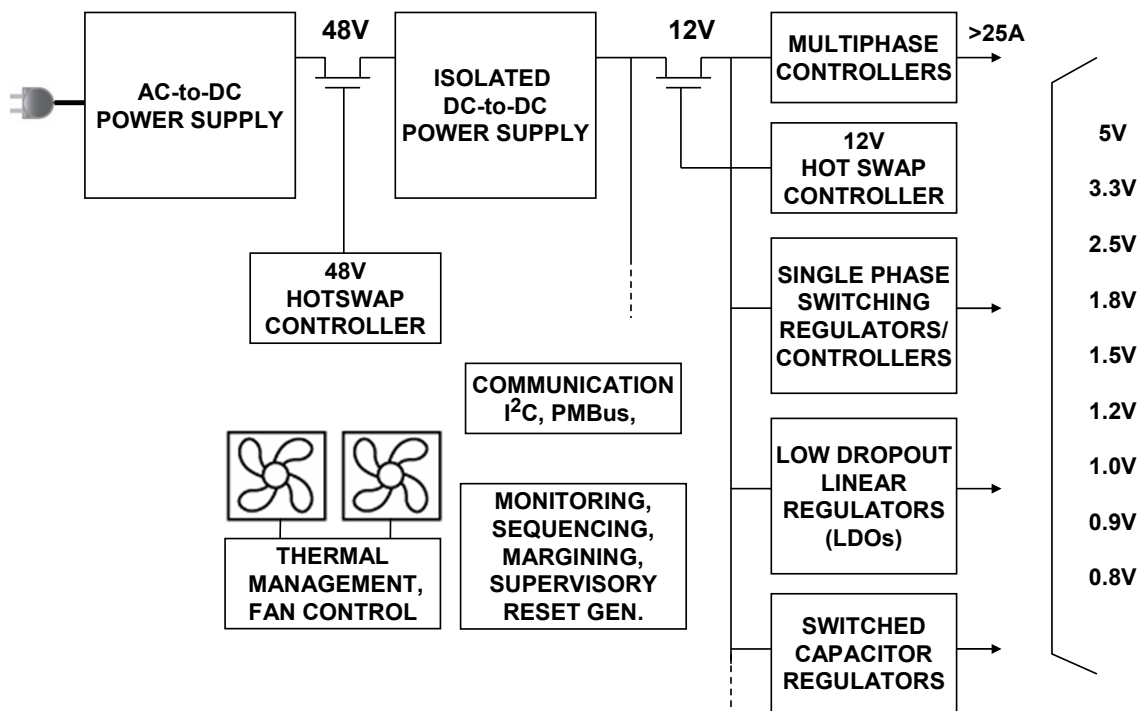
Devices in the system often require other regulated voltages, however, such as the core voltage for the processor. This voltage can be 0.8 V, 1.0 V, 1.2 V, 1.5 V, 1.8 V, etc. This requires a point-of-load (POL) regulated supply on the PC board specifically designed for the core voltage, which may be 10's of amps. The specific processor requirements often dictate other power supply requirements, such as load transient recovery, standby modes, etc.

The processor generally requires additional POL regulated voltages for the input/output (I/O) interface, and perhaps other auxiliary voltages.

Flexibility in the various voltages is important because of the trend toward ever faster, smaller geometry processes which require correspondingly lower core voltages.

One can easily see that it is both impractical and inefficient to generate these multiple voltage rails within the system power supply, and that POL regulation provides the best solution. In addition, local regulation generally provides "cleaner" voltage rails which is particularly important with low core voltages.

## Fixed Power Signal Chain Functional Blocks



This figure shows the typical functional blocks in the signal chain of a modern fixed power system.

The POL supplies can be either LDOs, single, or multiphase switched controllers, depending on the current output and efficiency requirements. The switched capacitor (also called charge pump, or "inductorless") regulator is also shown, but is more often associated with portable systems. (See Section 2 for further discussion of switched capacitor regulators).

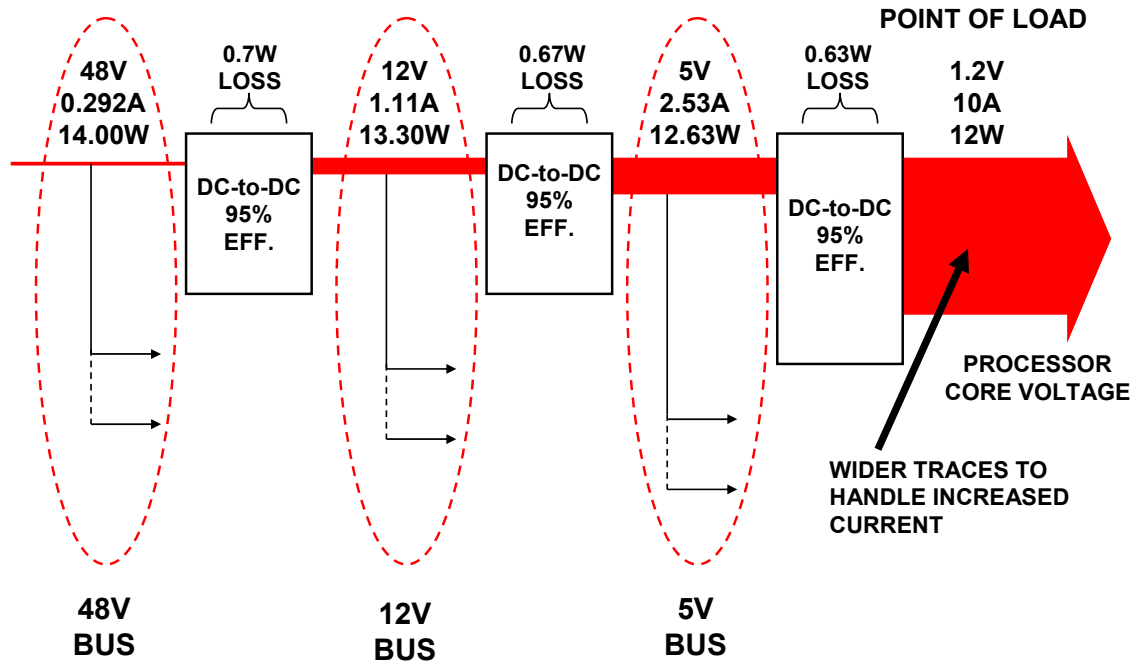
In addition to the POL regulators, there are also important auxiliary functions such as monitoring, sequencing, margining, and supervisory functions, such as power-on reset generators.

Thermal management and fan control is also an important part of modern power designs.

For telecommunications and server applications, hot swap controllers allow PC boards to be exchanged under power-on conditions.

A typical fixed power system may consist of some or all of the above functions, depending on the complexity and type of system.

## Intermediate Bus Structure and Point of Load Regulation Offer Flexibility and Efficiency



The use of intermediate bus structures and POL regulation offers both flexibility and efficiency as shown in this figure.

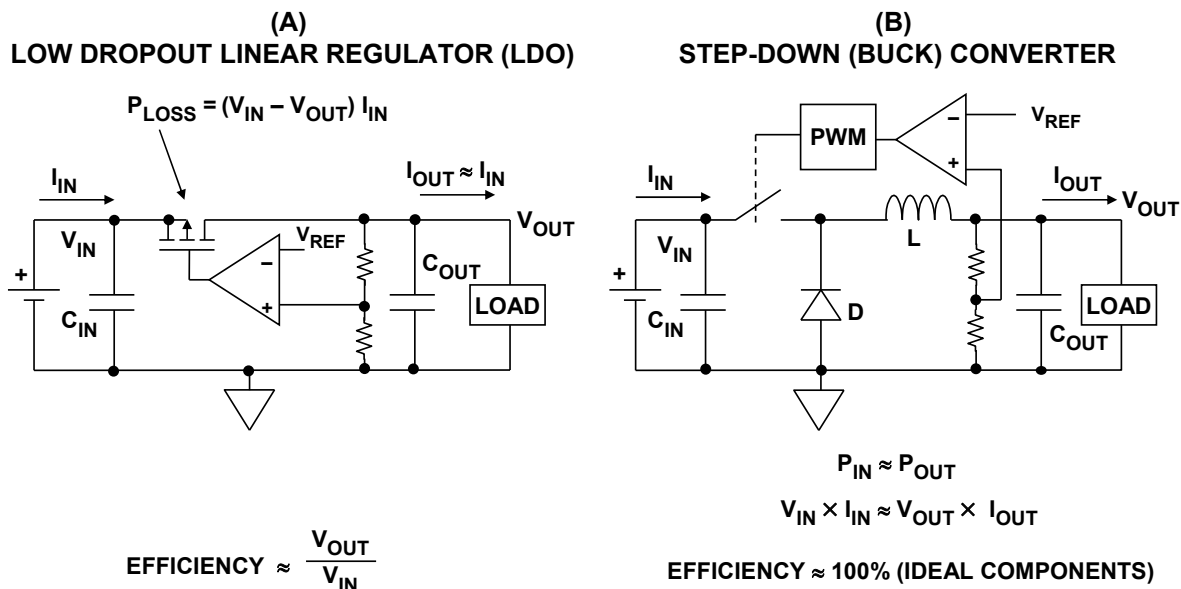
The path from the 48 V bus to the 1.2 V processor core is highlighted. In this example there are intermediate bus voltages of 12 V and 5 V which are distributed to other parts of the system.

It is assumed that the efficiency of each dc-to-dc converter is 95%. The power losses in the individual converters are shown. The only path shown is that for the processor core voltage. Additional currents supplied by each intermediate bus are not shown.

In order to maintain the same voltage drop in the PC traces, the trace width should be proportional to the amount of current carried. Note that POL regulation and the use of the intermediate bus architecture allow a short trace for the 10 A processor core current because the regulator is located close to the processor.

Further discussion of PC board layout issues can be found in Section 4.

## Two Popular Methods of Regulation: Linear and Switching



There are basically two types of POL regulators: linear and switching.

The linear regulator is the simplest type but generally the least efficient. However, linear regulators do not produce switching noise and ripple and are therefore useful in supplying power to sensitive analog components.

The power loss in a linear regulator is equal to the output current times the voltage dropped across the pass element (as shown in A). The efficiency is equal to the ratio of the output voltage divided by the input voltage, neglecting internal losses in the regulator, which should be relatively low.

Switching regulators, such as the buck (step-down) converter shown in B, transfer energy from input to output via an inductor that has the voltage polarity across it switching at a high frequency. If the circuit elements are ideal, the input power equals the output power, and the converter is 100% efficient. Regulation of the output voltage is achieved using a feedback loop which controls the duty cycle of the pulse width modulator (PWM), which in turn controls the on-time and off-time of the switching element, and hence the amount of energy transferred to the load.

Most popular switching regulators are based on magnetic elements, however the switched capacitor (or charge pump) regulator is often used in low current portable applications where the current requirement is less than approximately 200 mA. This type of regulator is discussed in more detail in Section 2.

## Linear Regulators vs. Switchers

<p>◆ <b>Linear Regulator Advantages</b></p> <ul style="list-style-type: none"> <li>● Simple low-cost design</li> <li>● Uses few external components; less board space required</li> <li>● No switching noise; low output ripple</li> </ul> <p>◆ <b>Disadvantages</b></p> <ul style="list-style-type: none"> <li>● Use only to generate a voltage lower than the input voltage</li> <li>● Efficiency <math>\approx V_{OUT} / V_{IN}</math></li> <li>● Power dissipation (heat rise) may be a concern</li> </ul> <p>◆ <b>Linear Regulator is best when</b></p> <ul style="list-style-type: none"> <li>● <math>V_{IN} - V_{OUT}</math> is small</li> <li>● Low-to-medium current applications</li> <li>● Low output ripple and noise are important</li> <li>● Space and cost are important</li> <li>● Powering sensitive analog circuits</li> </ul>	<p>◆ <b>Switching Regulator Advantages</b></p> <ul style="list-style-type: none"> <li>● Good for voltage increase, decrease, or inverting</li> <li>● High efficiency, 70% to 95%</li> <li>● Lower power dissipation</li> </ul> <p>◆ <b>Disadvantages</b></p> <ul style="list-style-type: none"> <li>● More complex and costly design</li> <li>● High output ripple</li> <li>● More components</li> </ul> <p>◆ <b>Switching Regulator is best when</b></p> <ul style="list-style-type: none"> <li>● <math>V_{IN} - V_{OUT}</math> is large</li> <li>● Low-to-high current applications</li> <li>● Efficiency is important</li> <li>● Voltage needs to be increased or inverted</li> </ul> <p>◆ <b>Switched Capacitor Regulators are suitable for some applications</b></p> <ul style="list-style-type: none"> <li>● Portable</li> <li>● Low currents (less than <math>\approx 200\text{mA}</math>)</li> </ul>
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The decision to use a linear or switching POL regulator is based on many factors. This table summarizes the key advantages and disadvantages of each type.

Linear regulators are certainly easier to use than switchers, require fewer external components, and occupy less board space. Linear regulators produce no switching noise and are often placed after a switching regulator to reduce the overall noise and ripple voltage. However, the PSRR of the linear regulator at the switching frequency must be carefully examined to determine its effectiveness in these applications.

The linear regulator is an excellent choice to power high performance analog circuits, such as ADCs, DACs, PLLs, DDS systems, data acquisition systems, instrumentation amplifiers, etc.

The chief disadvantage of the linear regulator is its efficiency, which is approximately  $V_{OUT}/V_{IN}$ . This may not be a problem for low output currents and low  $V_{IN} - V_{OUT}$  values, but can be a real concern at high output currents and larger  $V_{IN} - V_{OUT}$  values. Another concern is the power dissipation in the linear regulator at high output currents.

Most modern linear regulators use a low dropout (LDO) architecture which helps improve the efficiency. However, the switching regulator is the preferred choice in applications requiring high efficiency at high currents and large  $V_{IN} - V_{OUT}$  values.

Switching regulators definitely are more complex to design, require more components, and take up more board space. Extreme care must be taken in the layout in order to minimize ground bounce. Modern design tools are available from manufacturers such as Analog Devices' ADIsimPower™ to make the design process relatively painless, and allow optimization of various parameters such as efficiency, cost, and board space.

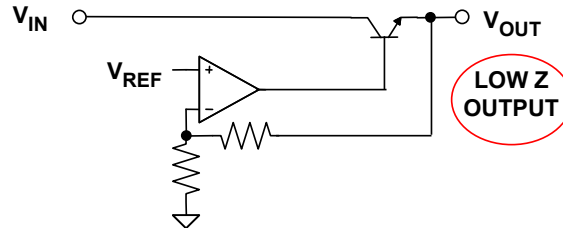
# Linear Regulators

[www.analog.com/ldo](http://www.analog.com/ldo)

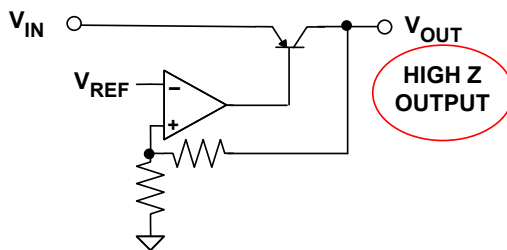


## Types of Linear Regulators

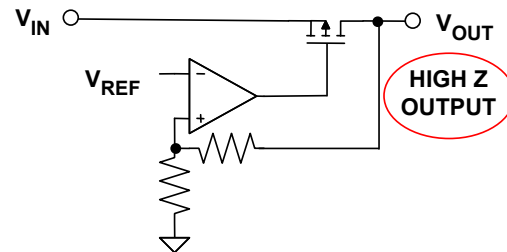
**(A) BIPOLAR REGULATOR  
WITH NPN EMITTER FOLLOWER**



**(B) PNP BIPOLAR LDO**



**(C) PMOS LDO**



These are the three fundamental types of linear regulators. All three architectures use a pass transistor, a voltage reference, and a feedback control loop to provide output voltage regulation.

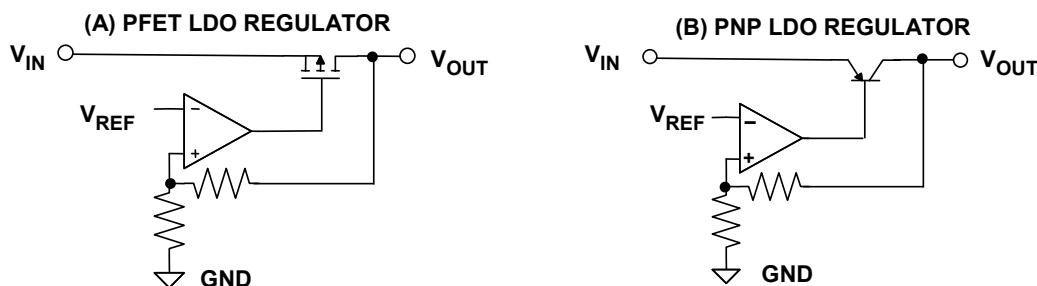
The circuit shown in (A) uses an NPN emitter follower as the pass device. Some NPN-based linear regulators use a darlington connection to reduce the base drive current. The advantage of this architecture is the inherently low output impedance and high bandwidth of the emitter follower which makes the regulator easy to stabilize under a variety of capacitive loads. The disadvantage of the NPN pass device is that the minimum value of  $V_{IN} - V_{OUT}$  (the dropout voltage) is approximately 1 V for the single NPN, and 2 V for the darlington connection.

It is possible to use an NMOS pass device, however an external bias voltage several volts greater than the input voltage is required in order to drive the gate. This can be a big disadvantage if such a voltage is not available.

The LDO circuit shown in (B) uses a bipolar PNP transistor as the pass device, and the dropout voltage can be as low as a hundred millivolts or so and is limited by the saturation voltage of the transistor,  $V_{CESAT}$ . The regulator maintains operation as long as the transistor is in its linear region. The disadvantage of this architecture is that the output impedance is high and the regulator is much more difficult to stabilize with bulk capacitive loads. Another disadvantage of using a bipolar process for the LDO is the larger amount of bias, or "ground current" required.

The circuit shown in (C) makes use of a PMOS pass device, and the dropout voltage is limited by the on-resistance of the FET. Like the circuit of (B), this circuit has a high open-loop output impedance and is more difficult to stabilize with bulk capacitive loads. The CMOS LDO has an advantage of extremely low "ground current". In addition, MOSFETs can be "sized" to supply reasonably high currents.

## PFET LDO vs. PNP LDO



### PFET/PNP LDO COMPARISON

- |                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>◆ Very low ground pin current does not increase with load</li> <li>◆ Dropout voltage can be very low as set by the ON-Resistance of the FET (<math>R_{ON}</math>)</li> </ul> | <ul style="list-style-type: none"> <li>◆ Ground pin current is higher: equals load current divided by beta (gain) of PNP transistor</li> <li>◆ Higher ground pin current wastes power.</li> <li>◆ Dropout voltage equals the saturation voltage of the PNP</li> </ul> |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

#### ADP1715, CMOS LDO

$I_{GND} @ 100\mu A = 100\mu A \text{ max}$

$I_{GND} @ 500mA = \underline{650\mu A \text{ max}}$

#### ADP3334, BIPOLAR LDO

$I_{GND} @ 100\mu A = 130\mu A \text{ max}$

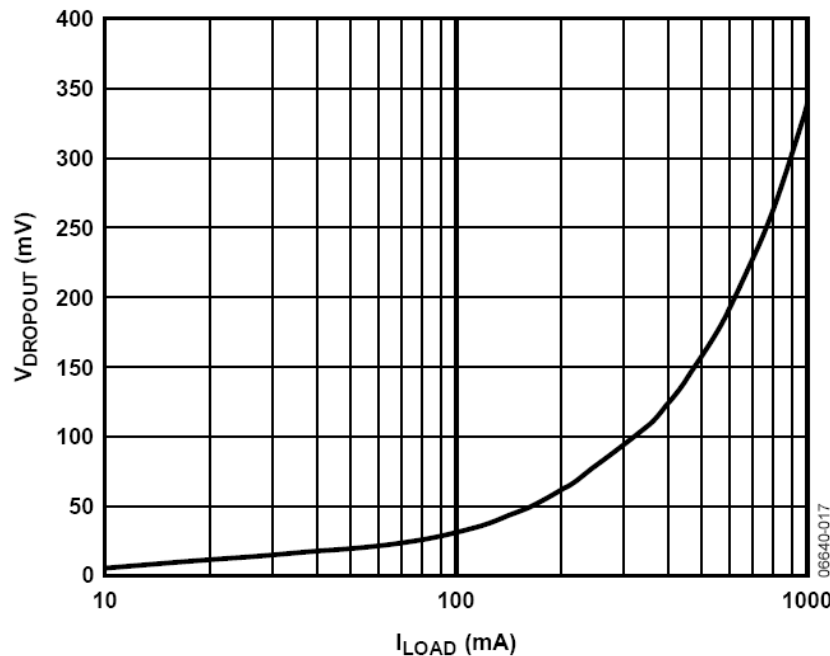
$I_{GND} @ 500mA = \underline{10mA \text{ max}}$

This shows a comparison between a typical PFET LDO (A) and a PNP LDO (B).

For a 500 mA load current, the ADP1715 CMOS LDO has a ground current of only 650  $\mu A$  compared to 10 mA for the ADP3334 bipolar LDO.

Most of the ground pin current in a PNP LDO is the current required to drive the base, which is equal to the load current divided by the beta of the PNP. Most bipolar processes do not support high beta PNP transistors.

## ADP1706/ADP1707/ADP1708 CMOS LDO Dropout Voltage vs. Load Current



The dropout voltage of a CMOS LDO can be made very low by designing for a low on-resistance. This shows the dropout voltage of the ADP1706/ADP1707/ADP1708 LDOs as a function of load current.

Note that the dropout voltage at 1 A is typically 345 mV.

The ADP1706/ADP1707/ADP1708 are CMOS, low dropout linear regulators that operate from 2.5 V to 5.5 V and provide up to 1 A of output current. Using an advanced proprietary architecture, they provide high power supply rejection and achieve excellent line and load transient response with a small 4.7  $\mu$ F ceramic output capacitor.

The ADP1706/ADP1707 are available in 16 fixed output voltage options. The ADP1708 is available in an adjustable version, which allows output voltages that range from 0.8 V to 5.0 V via an external divider. The ADP1706 allows an external soft start capacitor to be connected to program the start-up time; the ADP1707 and ADP1708 contain internal soft start capacitors that give a typical start-up time of 100  $\mu$ s. The ADP1707 includes a tracking feature that allows the output to follow an external voltage rail or reference.

The ADP1706/ADP1707/ADP1708 are available in an 8-lead, exposed paddle SOIC package and an 8-lead, 3 mm  $\times$  3 mm exposed paddle LFCSP, making them not only very compact solutions but also providing excellent thermal performance for applications requiring up to 1 A of output current in a small, low profile footprint.

## Linear Regulator Specifications

- ◆ **Drop-Out Voltage**
  - Defined as the minimum Input to Output Differential Voltage required to maintain the output voltage within 100mV of the nominal value
  - This specification directly translates to efficiency and battery life
- ◆ **Ground Current (bias current)**
  - The current required by the regulator itself to operate over the full load range. Sometimes called quiescent current ( $I_Q$ ).
  - Will vary with load current
  - Directly translates to efficiency, especially at light loads
- ◆ **Power Supply Rejection Ratio (PSRR)**
  - The ratio of output voltage change due to a change in the input voltage
  - This must be examined at the specific ripple frequency when using the LDO as a "ripple filter"
- ◆ **Regulator Output Error**
  - The output voltage deviation from the nominal or ideal value

This figure summarizes the key linear regulator specifications. It is common to specify total output accuracy as a percentage.

Note that many applications depend on the linear regulator to "filter" a switching regulator output. Extreme caution must be exercised in these applications to filter as much of the high frequency noise as possible BEFORE it enters the linear regulator. The PSRR of linear regulators at high frequencies is generally not sufficient to properly filter these transients.

In addition, carefully examine the PSRR of the linear regulator at the switching frequency of interest to make sure it is sufficient.

## Regulator Output Error

- ◆ **Regulator Output voltage error is a combination of:**
  - **Line regulation ability** (maintain a nominal output voltage with varying input voltage,  $\Delta V_{OUT} / \Delta V_{IN}$ )
  - **Load regulation ability** (maintain a nominal output voltage with varying load currents,  $\Delta V_{OUT} / \Delta I_{OUT}$ )
  - **Internal Reference and Amplifier errors** due to temperature and voltage changes
- ◆ **Total error is expressed as a percentage of the nominal output voltage, usually from 1% to 3%**
- ◆ **Early bipolar regulators were generally more accurate than CMOS regulators due to having better internal references. Today, the distinction is minimal**

This figure defines the total regulator output voltage error. Total error generally is between 1% and 3%.

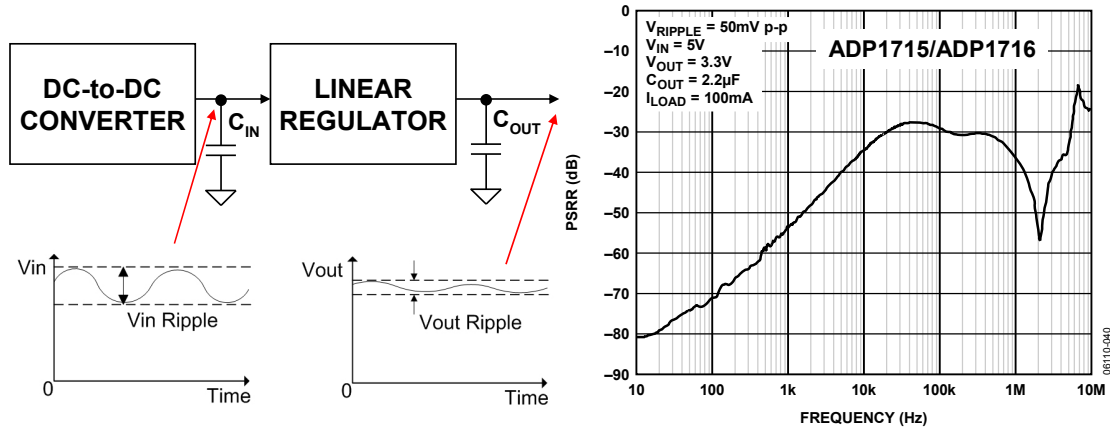
Early bipolar regulators were generally more accurate than their CMOS counterparts because of better internal voltage references. Today this distinction is minimal, and both technologies are capable of 1% accuracy.

There are two considerations regarding accuracy. The first is the absolute accuracy of a regulator. Ultimately this value should be traceable to a reference standard. In a practical regulator, accuracy is a function of input voltage (line regulation) and the load current (load regulation). The second is the drift due to temperature or ageing.

In most systems the initial accuracy errors can be removed by calibration, and the drift due to temperature or ageing are more important.

## LDO Power Supply Rejection

- ◆ Power supply rejection ratio is a measure of how well a circuit rejects ripple at various frequencies coming from the input power supply
- ◆ Comparing ratio of output ripple to input ripple
- ◆ PSRR is expressed in dB, and is plotted on a log scale of dB vs. Frequency
- ◆ Frequency range of interest is usually 10Hz to 10MHz
- ◆ Devices with good PSRR typically have high gain and a high unity gain frequency
- ◆ High PSRR devices are sometimes used for post regulation of DC-to-DC converters



As previously mentioned, LDOs are commonly used to reduce the ripple from a switching regulator. In these applications, the PSRR of the LDO must be examined at the specific switching frequency of the switching regulator. LDO PSRR is typically shown from 10 Hz to 10 MHz.

The figure shows the PSRR (in dB) of the ADP1715/ADP1716 500 mA CMOS LDO as a function of frequency for a load current of 100 mA with a 2.2  $\mu\text{F}$  ceramic output bulk capacitor.

Any good quality ceramic capacitors can be used with the ADP1715/ADP1716, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics. More discussion of capacitors can be found in Section 4.

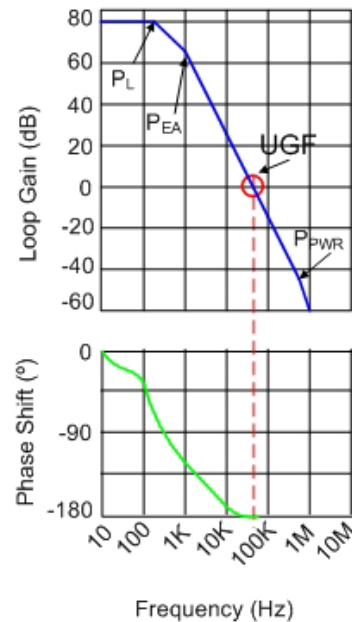
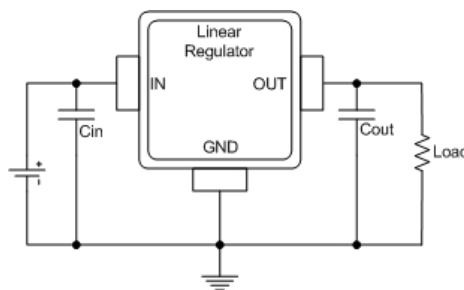
The PSRR curves show a characteristic "dip" at high frequencies. The start of the dip is due to the attenuating effect of the output bulk capacitor. However, the curve starts to rise again because of the output capacitor ESL. The "depth" of the dip is determined by the output capacitor ESR.

At high frequencies, (greater than approximately 10 MHz), the output capacitor and its characteristics dominate the PSRR. This illustrates the importance of localized decoupling at the power pins of each IC in addition to providing sufficient bulk capacitance at the LDO output to attenuate the lower frequency components.

In addition, sufficient capacitance is required at the LDO input to filter high frequency components

## Stability Issues with Traditional PNP or PMOS LDOs

- ◆ **Regulators with PNP or PMOS pass devices have several Poles around the control loop:**
  - **Low frequency Pole due to the output capacitor and the load resistance ( $P_L$ )**
  - **Low frequency Pole due to the error amplifier compensation ( $P_{EA}$ )**
  - **High frequency Pole due to the power pass device ( $P_{PWR}$ )**
- ◆ **Low frequency Poles are dominant and cause  $180^\circ$  of negative phase shift in the loop before the 0dB point (Instability)**

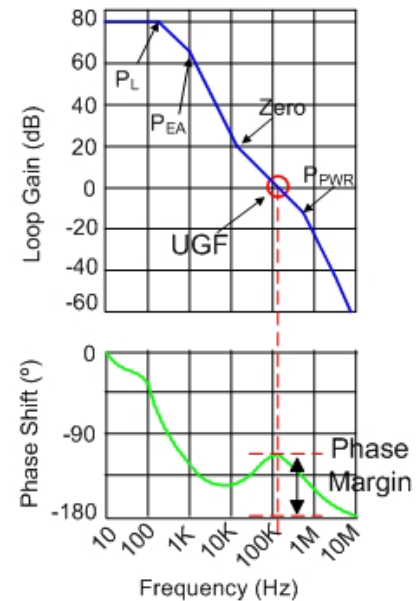
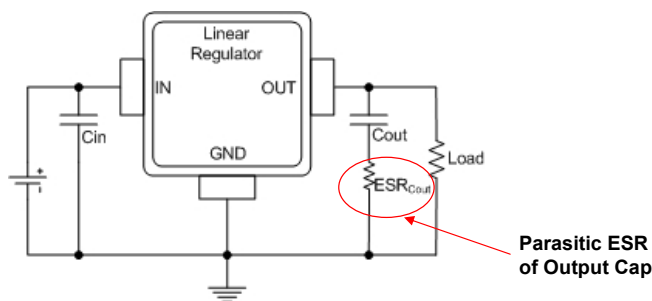


Traditional LDOs designed with PNP or PMOS pass devices have several poles around the control loop as shown. The first is labeled  $P_L$  and is due to the output capacitor and the load resistor. The second pole,  $P_{EA}$ , is due to the internal error amplifier compensation. There is an additional high frequency pole,  $P_{PWR}$ , due to the power pass device.

Note that the two low frequency poles,  $P_L$  and  $P_{EA}$ , cause  $180^\circ$  of phase shift at the point of unity gain, and therefore the system as shown is unstable.

## Stabilizing the Regulator Loop Using the Zero Created by the Output Capacitor and its ESR

- ◆ A Zero is needed to cancel the phase shifting effect of one of the low frequency poles
- ◆ Designers make use of the parasitic ESR of the output cap to provide this necessary low freq Zero.
- ◆ A well placed Zero will add positive phase shift to the loop and therefore make it stable
- ◆ Zero also increases the loop bandwidth (higher 0dB point), Beware!



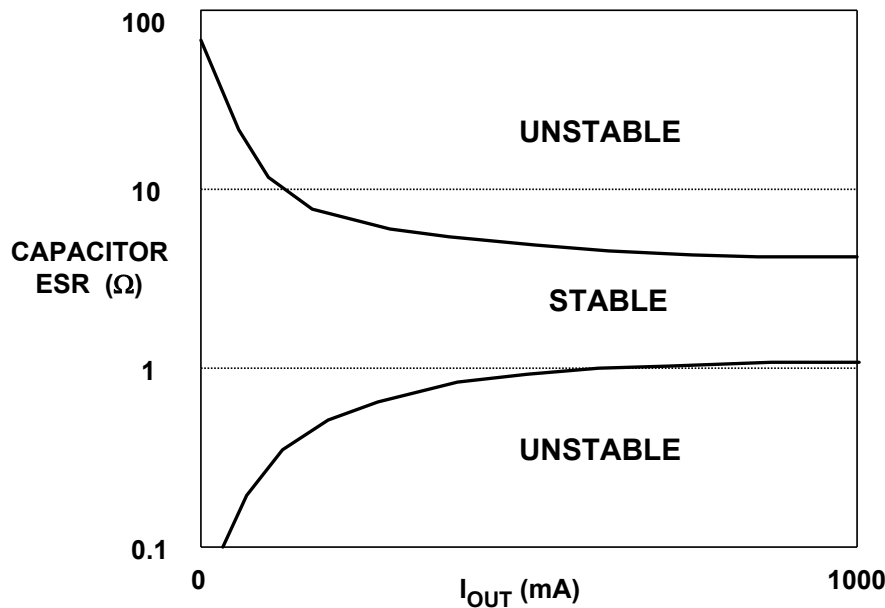
An external zero is needed to cancel the phase shift of one of the low frequency poles. LDO designers have often used the parasitic ESR of the output capacitor to provide this necessary low frequency zero as shown in the above figure.

However, the additional zero must be placed at the correct frequency and will also increase the loop bandwidth.

This results in a "zoned" ESR requirement on the external bulk capacitor. Relying on this approach for stabilization is risky because ESR may not be repeatable from capacitor to capacitor. There can be additional distributed decoupling capacitors located at individual ICs which create more variables.



## Zoned Load Capacitor ESR Can Create an LDO Applications Nightmare



A typical PNP or PMOS LDO using traditional designs has an allowable range of bulk capacitor ESR values which will ensure stability. The ESR value is also a function of the load current.

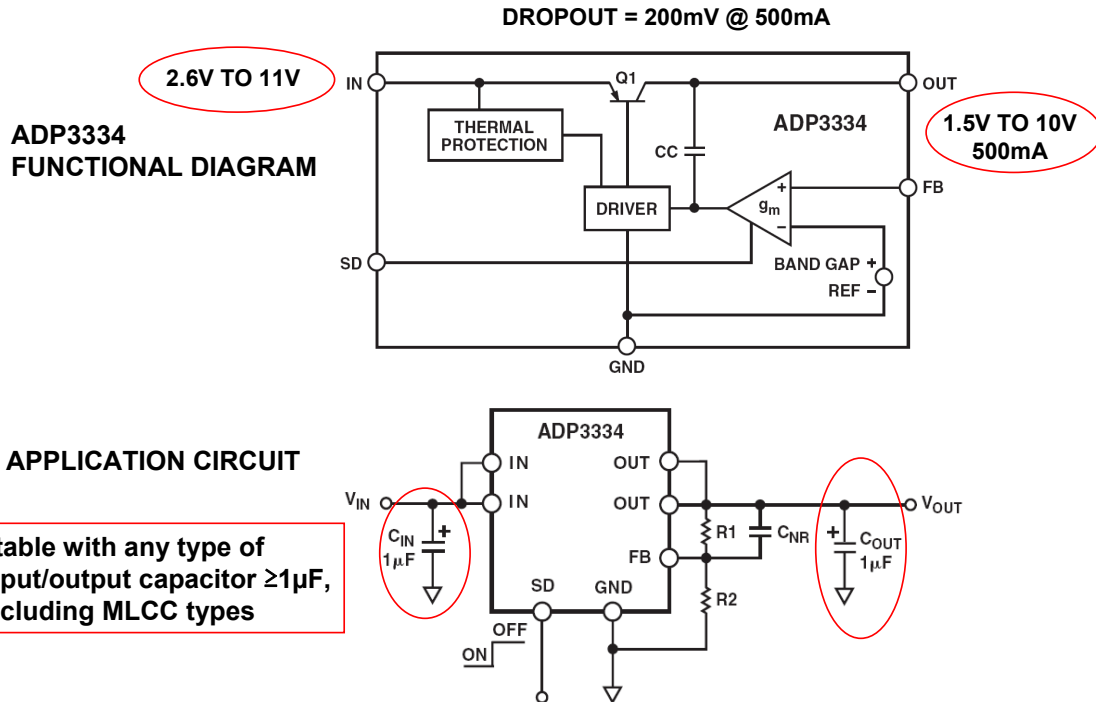
The "zoned" ESR requirement on the external capacitor is an applications nightmare because the engineer is relying on a parasitic parameter for stability.

A zoned ESR chart such as this is meant to guide the user of an LDO in picking an output capacitor which confines ESR to the stable region, i.e., the central zone, for all operating conditions. Note that this generic chart is not intended to portray any specific device, just the general pattern. Unfortunately, capacitor facts of life make such data somewhat limited in terms of the real help it provides. Bearing in mind the requirements of such a zoned chart, it effectively means that general purpose aluminum electrolytic are prohibited from use, since they deteriorate in terms of ESR at cold temperatures.

Very low ESR types such as OS-CON or multilayer ceramic units have ESRs which are too low for use. While they could in theory be padded up into the stable zone with external resistance, this would hardly be a practical solution.

This leaves tantalum types as the best all around choice for LDO output use where "zoned" ESR is required. Finally, since a large capacitor value is likely to be used to maximize stability, this effectively means that the solution must use a more expensive and physically large tantalum capacitor. This is not desirable if small size is a major design criteria.

## Bipolar LDOs Use anyCAP Design



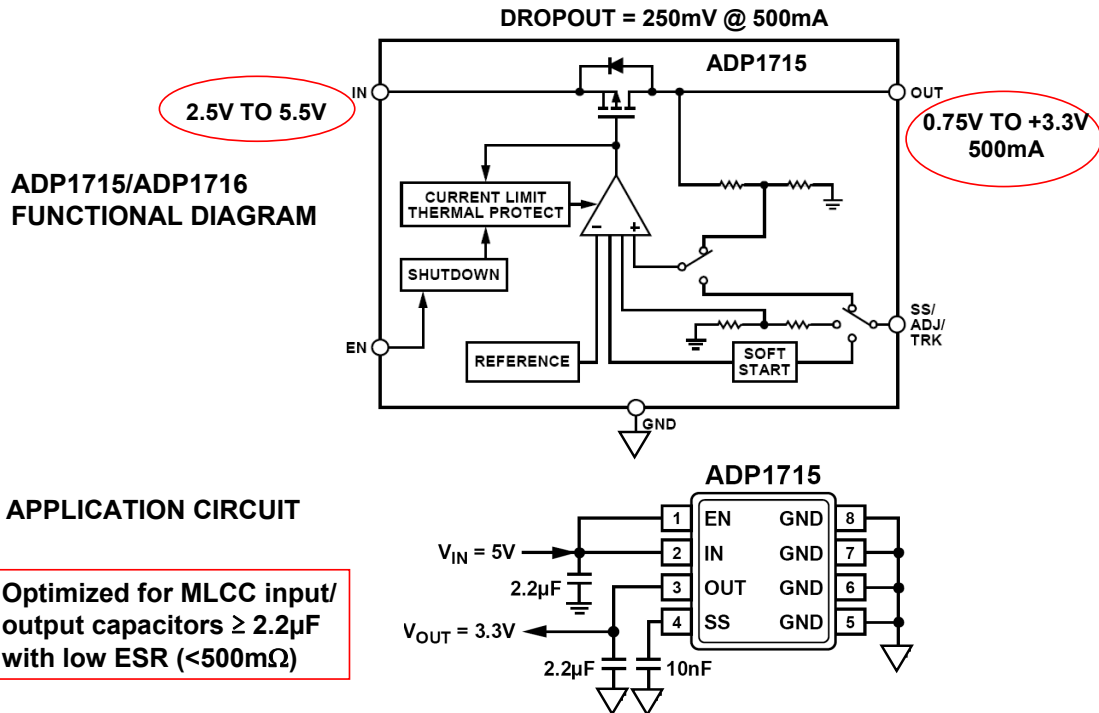
The Analog Devices' family of anyCAP bipolar LDOs, introduced in the mid-1990s, pioneered the use of a different control loop topology which removed the "zoned" ESR requirement on the external bulk capacitor. This family is stable with any type of input/output capacitor greater than 1  $\mu\text{F}$ , including the low ESR multilayer ceramic (MLCC) types.

This figure shows the functional diagram of the series as well as a typical application circuit.

A detailed description of the anyCAP design is found in the following reference:

Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273 Chapter 7. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410, Chapter 7.

## Analog Device's CMOS LDOs



As was previously mentioned, CMOS LDOs provide low on-resistance PFET pass devices as well as low quiescent (ground) current. Advances in voltage reference technology now allow CMOS LDOs to match the accuracy of bipolar LDOs.

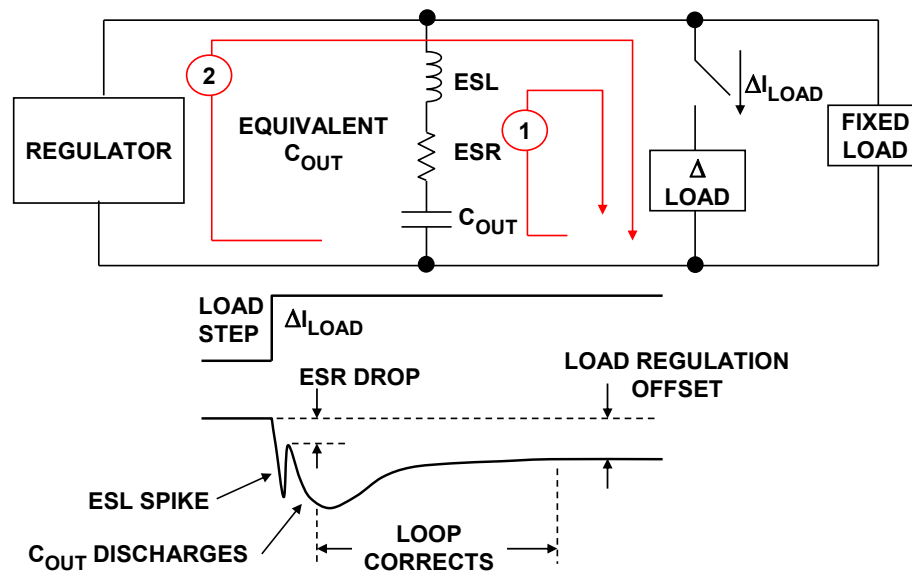
The ADP1715/ADP1716 family of CMOS LDOs are designed for operation with small, space-saving ceramic capacitors, but they will function with most commonly used capacitors as long as care is taken about the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 2.2  $\mu\text{F}$  capacitance with an ESR of 500 m $\Omega$  or less is recommended to ensure stability of the ADP1715/ADP1716.

Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1715/ADP1716 to large changes in load current.

Any good quality ceramic capacitors can be used with the ADP1715/ADP1716, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

This figure shows a block diagram of the ADP1715 500 mA CMOS LDO and a typical application circuit. The external 10 nF capacitor provides a soft-start time of approximately 7 ms.

## Transient Response to Current Load Step



- ◆ (1)  $C_{OUT}$  must supply initial current to load during the first few microseconds after switch closes.
- ◆ (2) Then the regulator loop takes over and eventually supplies all the static load current

Transient response to a current load step is important, especially when the LDO is powering a digital device with widely varying load currents, such as an FPGA or DSP.

In many cases, the core allowable voltage tolerance specification includes not only the static voltage error but also transient error. Exceeding these limits under either static or transient conditions can cause erratic operation of the DSP, FPGA, or other processor. For example, a total tolerance of  $\pm 5\%$  is common on the core voltage for an FPGA. For a 1.2 V core voltage, the total allowable error is therefore only  $\pm 60$  mV.

This figure shows a typical load transient response to a load step in current.

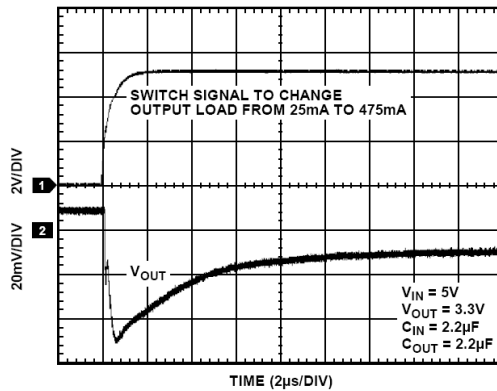
Before the application of the load step, the LDO supplies all the static load current.

Immediately after the application of the load step, the output capacitor must supply all of the transient current as shown in the loop labeled "1". There is an initial voltage drop due to the capacitor ESR which is followed by an inductive spike due to the capacitor ESL. The capacitor then begins to discharge into the load for a few microseconds until the LDO feedback loop begins to correct for the load current change.

As the feedback loop continues to correct (shown in the loop labeled "2"), the output voltage settles to a final value which is determined by the load regulation of the LDO. At this point, the LDO once again supplies all the static load current.

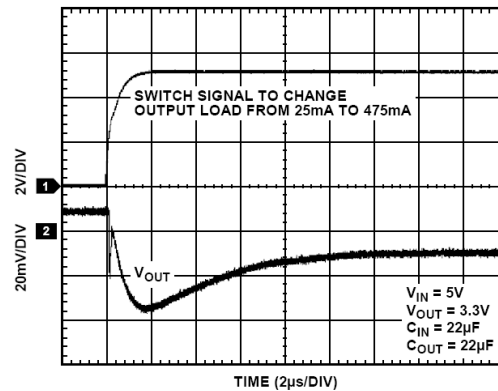
It is important to remember that the total output capacitance also includes the distributed localized capacitors at the various ICs which make up the load as well as PC board parasitics.

## Linear Regulator Load Current Step Transient Response for ADP1715/ADP1716



$$C_{IN} = C_{OUT} = 2.2\mu F$$

TRANSIENT = 60mV, or 1.8%



$$C_{IN} = C_{OUT} = 22\mu F$$

TRANSIENT = 45mV, or 1.4%

This figure shows the load current step transient response of the ADP1715/ADP1716 CMOS LDO for a load step change from 25 mA to 475 mA. The input voltage to the LDO is 5 V, and the output voltage is 3.3 V.

The left-hand response is for an input and output MLCC capacitor of 2.2  $\mu$ F, and the right-hand response is for a 22  $\mu$ F input and output capacitor. The transient amplitude is 60 mV (1.8%) and 45 mV (1.4%), respectively.

The lack of ringing in the transient response indicates good stability and phase margin for the LDO control loop.

The transient response is also a function of the amplitude of the current step. Small current steps produce less initial voltage drop across the output capacitor ESR, but the total transient settling time is dependent on the control loop and its compensation and may not reduce proportionally.

## Other Useful Features for Low Dropout Linear Regulators

- ◆ **Adjustability**, use of external resistors to set the nominal output voltage
- ◆ **Enable Pin**, to externally control when the regulator turns on and off
- ◆ **Soft-Start**, controls the rise time of the output voltage during power-up, thus limiting inrush current
- ◆ **Tracking Feature**, external voltage rail can be fed into the regulator, the output will track this external voltage
- ◆ **Error Pin**, indicates when output is about to go out of regulation
- ◆ **Overcurrent Protection**, limits the output current
- ◆ **Thermal Shutdown**, turns the regulator output off if the junction temperature rises above 150°C
- ◆ **Noise Reduction**, allows external bypassing of the regulator's reference voltage, thus reducing noise on the output rail

Modern LDOs are available with many features which greatly aid in their application. This figure lists a few.

In some applications it is desirable to set the output voltage to a specific value using external resistors.

The *Enable* function can be used to externally control when the regulator turns on and off, and the *Soft-Start* function can control the rise time of the output voltage during power-up thus limiting the inrush current.

The *Soft-Start* feature is especially important when powering devices such as FPGAs which require a monotonic ramp-up of voltage. When the regulator output voltage begins to rise, the regulator must supply current to charge the total output bulk capacitance ( $I = C \times dv/dt$ ) as well as the current required by the load. If the sum of these currents is greater than the current limit of the regulator, the output will become non-monotonic. Accurate control of the ramp-up time ( $dv/dt$ ) is therefore critical in this type of application.

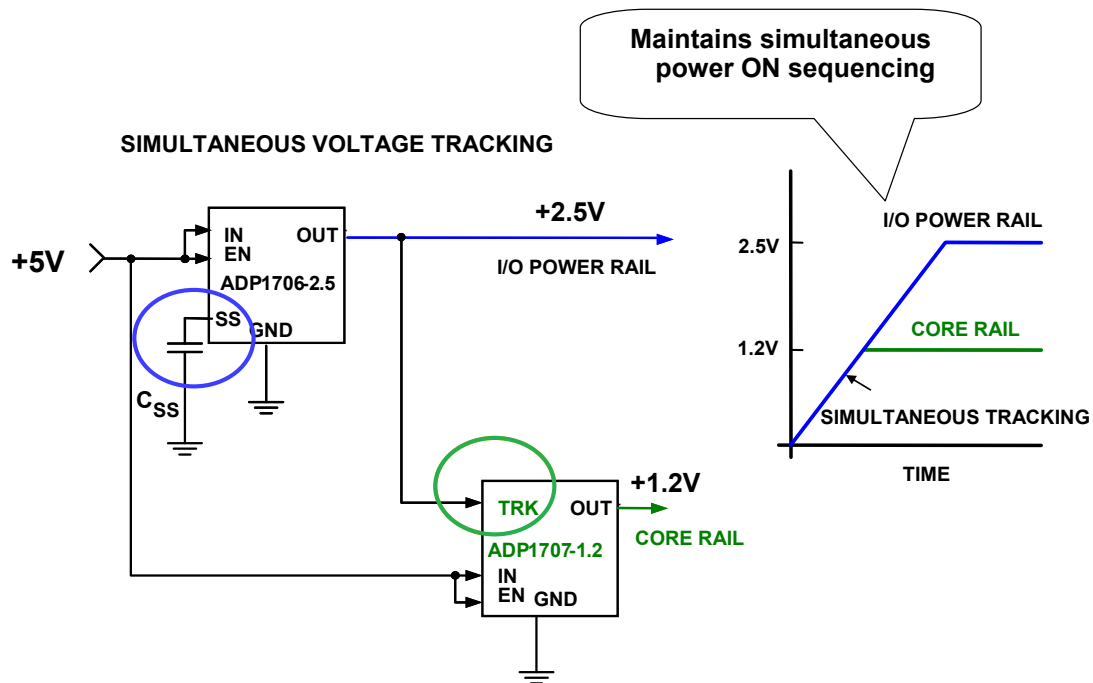
A *Tracking* feature is useful in performing simple sequencing functions between regulators.

An *Error* function pin indicates when the output is about to go out of regulation.

*Overcurrent* and *Thermal Shutdown* features protect downstream circuitry as well as the LDO.

The addition of a *Noise Reduction* pin allows external bypassing of the regulator's internal reference voltage, thereby reducing noise on the output.

## ADP1707 Simultaneous Voltage Tracking



Simple sequencing and power-on issues can be resolved by utilizing the Soft-Start, Enable, and Tracking functions available on new LDOs such as the ADP1706, ADP1707, and ADP1708 family of 1 A CMOS regulators.

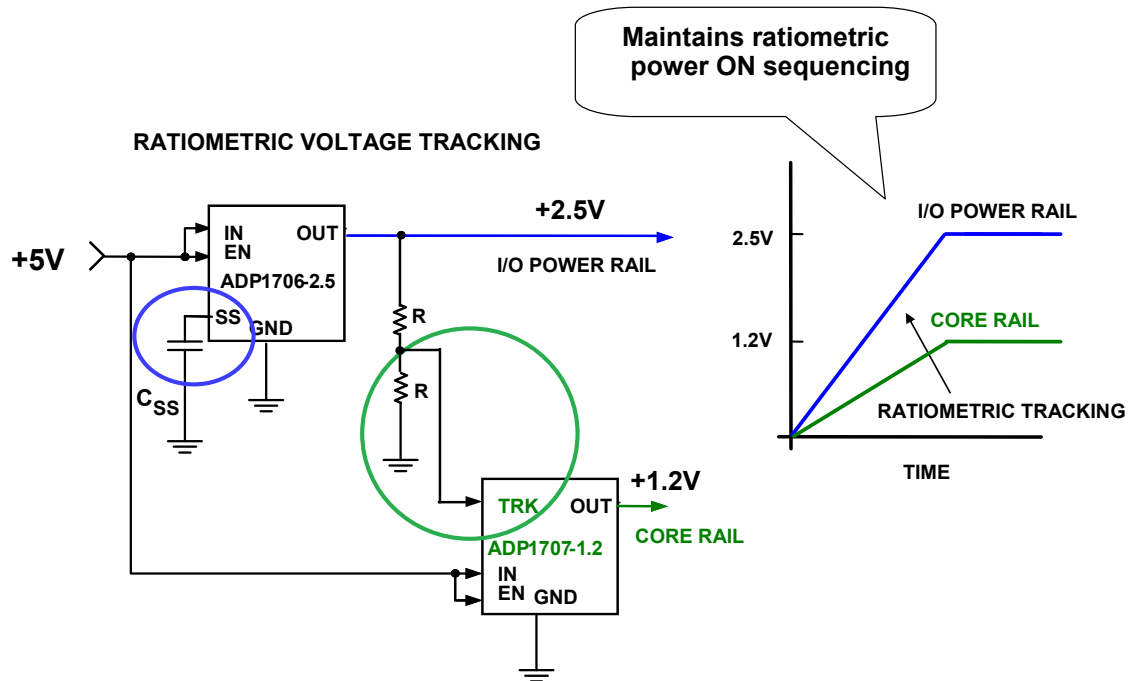
All parts in the family have an Enable function. The three parts are differentiated by the function assigned to Pin 8. The ADP1706 has a Soft-Start function (SS) on Pin 8 which can be programmed using an external capacitor, the ADP1707 has an internal Soft-Start function which gives a typical start-up time of 100  $\mu$ s. The ADP1707 has a Tracking function (TRK) assigned to Pin 8 that allows the output to follow an external voltage rail or reference.

The ADP1706 and ADP1707 come in 16 fixed output voltage options, while the ADP1708 output voltage is adjustable from 0.8 V to 5.0 V by connecting the appropriate external resistor between Pin 7 and Pin 8.

In the application shown in this figure, it is desired to bring up the 2.5 V I/O power rail and the 1.2 V core power rail simultaneously upon the application of the 5 V rail and the Enable function. The 2.5 V I/O start-up ramp slope is controlled by the external capacitor connected to the Soft-Start (SS) pin of the ADP1706-2.5. The Soft-Start time is calculated by  $T_{SS} = V_{REF} \times (C_{SS}/I_{SS})$ , where  $V_{REF} = 0.8$  V, and  $I_{SS} = 1.2$   $\mu$ A. For  $C_{SS} = 10$  nF,  $T_{SS} \approx 7$  ms.

The output of the upper 2.5 V I/O regulator (ADP1706-2.5) is applied to the Tracking input of the lower 1.2 V core regulator (ADP1707-1.2) which forces the output of the 1.2 V core regulator to track the output of the 2.5 V I/O regulator. This provides the desired simultaneous tracking as shown.

## ADP1707 Ratiometric Voltage Tracking



In this figure, the particular processor requires ratiometric sequencing as shown.

Ratiometric sequencing is easily implemented using a circuit very similar to the previous figure, except here the Tracking input of the 1.2 V core regulator is driven by the attenuated ( $\div 2$ ) output of the 2.5 V I/O regulator.

If the voltage applied to the TRK pin is less than the nominal output voltage, the output voltage is equal to the voltage at TRK. Otherwise, the output voltage is regulated to its nominal output value. In this example, the 1.2 V core regulator begins to regulate when the I/O voltage reaches 2.4 V.

It should be noted that the sequencing and power-up requirements differ widely between various FPGAs, DSPs, etc., and the examples shown in the last two figures are only shown to illustrate two possible arrangements.



# Switching Regulators and Controllers

[www.analog.com/regulators](http://www.analog.com/regulators)

[www.analog.com/controllers](http://www.analog.com/controllers)

[www.analog.com/adisimpower](http://www.analog.com/adisimpower)

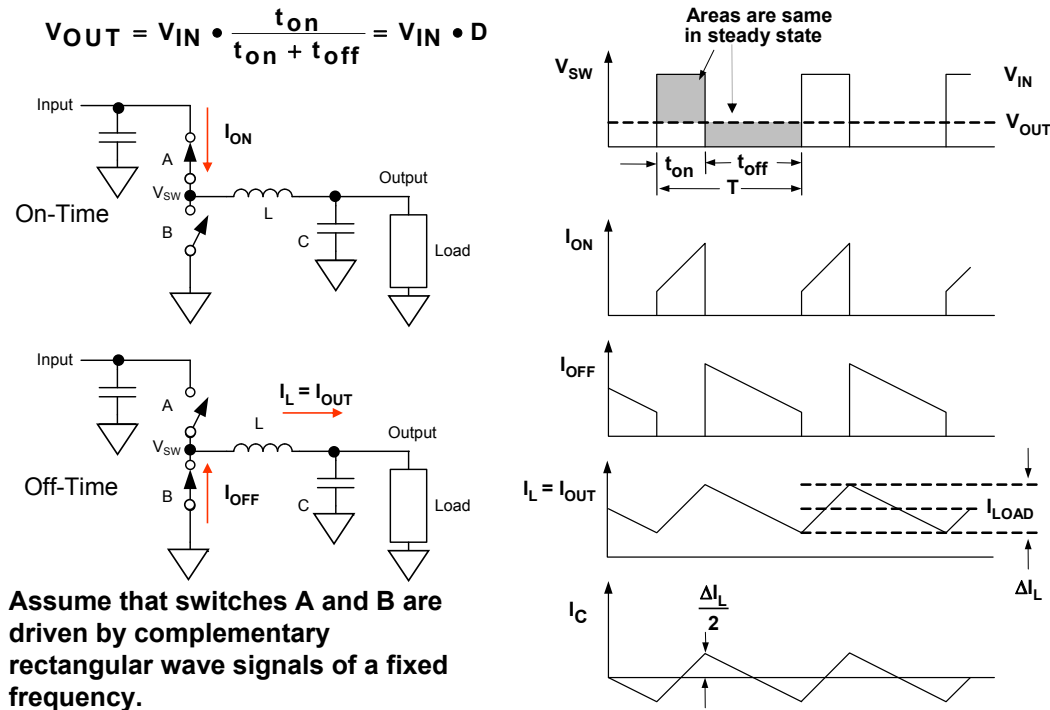
Soon after the invention and proliferation of the integrated circuit, system designers were somewhat successful in standardizing on a few popular voltages. For instance, the analog circuits typically ran on  $\pm 15$  V or  $\pm 12$  V supplies, and the digital logic on +5 V. The design of the "system power supply" (silver box) was relegated to the reclusive "power supply designer," and the voltages from the central power supply were distributed over the wiring and the backplane to the various system PC boards which were most often designed by other engineers.

Although a "silver box" equivalent still exists in most systems, this simple design philosophy has been complicated by the need for "intermediate" supply busses and point-of-load regulation. This is largely due to the proliferation of multiple rails, the trend toward lower power and lower voltages, and many other factors. Modern design engineers working at the PC board level must therefore be competent in the application of both linear and switching regulators in order to complete their designs. The silver box "guru" may not be amenable to designing the local 10 A supply for the 1.2 V FPGA core voltage.

Like the linear regulator, the magnetic switching regulator has become a fundamental building block in today's point-of-load applications, primarily because of its efficiency and flexibility. Fortunately, a complete theoretical understanding of the various intricacies of switching regulator design is not required in order to successfully apply them.

The concepts presented in the following section along with appropriate design tools (ADIsimPower) and application support should certainly make the design of the switching regulator less daunting to modern PC board designers. Textbooks and other reference material abound for those wishing to obtain a deeper understanding.

## Step-Down (Buck) Converter



This shows the basic operation of a buck, or step-down, converter. If all circuit elements are ideal there is no power loss, and the circuit is 100% efficient. The input power is equal to the output power:  $P_{IN} = P_{OUT}$ , and therefore  $V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT}$ .

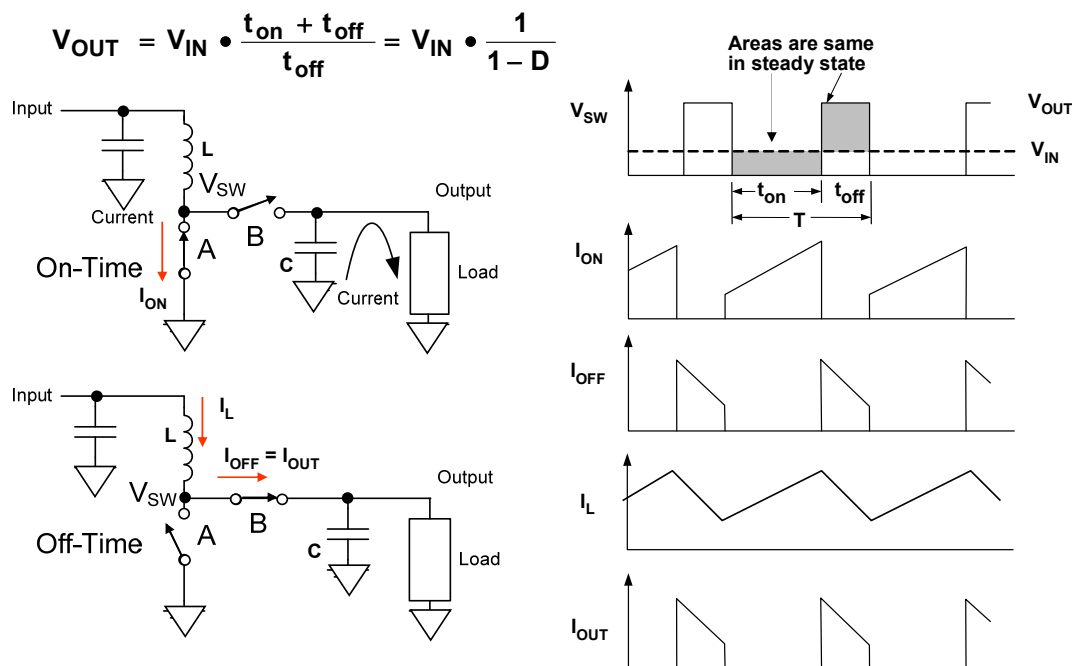
The switches are driven by complementary rectangular wave signals of a fixed frequency, but varying duty cycle (i.e., pulse width modulation, or PWM). During the "on-time" cycle when switch A is closed, there is a positive voltage dropped across the switching inductor causing current through it to ramp up linearly and store energy in the inductor's magnetic field. During the "off-time" cycle when switch B is closed, there is a negative voltage dropped across the inductor causing the current to ramp down linearly and releasing the energy stored in the inductor as it is transferred to the load.

The output voltage is equal to the input voltage multiplied by the duty cycle,  $D$ , of the PWM signal ( $V_{IN} \times D = V_{OUT}$ ). The duty cycle is defined as the percentage of time of the total switching period that switch A is closed. The output voltage is regulated by a feedback loop which senses the output voltage, compares it to a fixed reference, and adjusts  $D$  accordingly. This method of control is called "voltage mode" control (VMC). Another popular control technique is "current mode" control (CMC) which uses an additional feedback loop which senses the inductor current as well.

The output capacitor (also called the "bulk" capacitor) acts in conjunction with the inductor to filter the voltage waveform at the switch node,  $V_{SW}$ . In addition, it must be able to handle the ripple current which is typically 20% to 30% of the static output current. The output ripple voltage magnitude is a function of the output capacitance, its parasitic equivalent series resistance (ESR), and the PCB parasitic impedances. In the normal operation of a buck converter, the output current is continuous, and the input current is discontinuous. This generally implies that additional filtering on the input is required in order to prevent EMI/RFI problems.

Note that as the load current decreases, it is possible for the inductor current to go to zero if switch B is unidirectional. This is called the "discontinuous" mode as opposed to the "continuous" mode when the inductor is always conducting.

## Step-Up (Boost) Converter



The step-up or boost converter is rarely used in fixed power POL applications, because of the advantages previously discussed of always stepping down in voltage. The boost converter finds its primary use in portable equipment where the battery voltage is not great enough to power part or all of the electronics.

The basic boost converter shown here uses two switches and an inductor. The topology simply switches the position of the input and output to that of a buck converter. The result is a configuration which provides an output voltage which is greater than the input voltage. If all circuit elements are ideal there is no power loss, and the circuit is 100% efficient (practical circuits with real losses can approach 95% with careful design). The input power is equal to the output power:  $P_{IN} = P_{OUT}$ , and therefore  $V_{IN} \times I_{IN} = V_{OUT} \times I_{OUT}$ . This can mean very large input currents for large  $V_{OUT}/V_{IN}$  ratios.

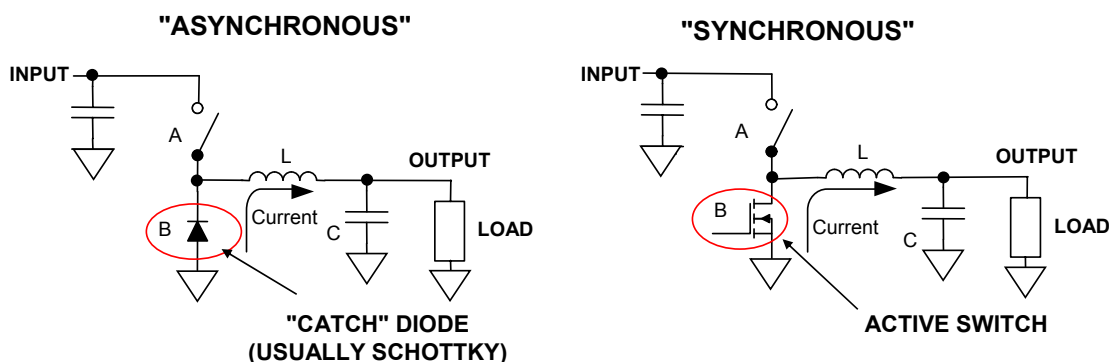
As in the buck converter, the boost converter switches are driven by two complementary PWM waveforms whose duty cycle determines the output voltage. The duty cycle is controlled by sensing the output voltage, comparing it to a known reference, and adjusting the duty cycle,  $D$ , accordingly. The relationship between the input and output voltages and  $D$  is given by  $V_{OUT} = V_{IN} / (1 - D)$ . Duty cycle ( $D$ ) is defined as the percentage of time of the total switching period that switch A is closed.

During the "on-time" cycle when switch A is closed, the voltage across the inductor is equal to the input voltage, and the inductor current ramps up linearly as energy is stored in its magnetic field. Also during the "on-time" cycle, the bulk capacitor and the load are disconnected from the converter, the capacitor must supply the load current. During the "off-time" cycle when switch B is closed, there is a negative voltage dropped across the inductor equal to the output voltage minus the input voltage causing the inductor current to ramp down linearly as energy is delivered to the load via the inductor.

Unlike the buck converter, the boost converter has a discontinuous output current and a continuous input current. Output filtering requirements for the boost converter are therefore more stringent than in the buck converter, although the input to the boost converter is more benign.

## DC-to-DC Converter Terminology:

- ◆ **Switching Regulator:** Switches are Internal (<5A)
- ◆ **Switching Controller:** Switches are External (0.1A to 40A)
- ◆ **Multiphase Switching Controllers:** Switches are External (About 40A / phase)



It is important to define some general terminology relating to dc-to-dc converters. Although these are widely accepted industry definitions, there may be some variation in usage between manufacturers.

The term switching *Regulator* implies that the switches are internal to the IC. These types of converters are typically limited to less than 5 A output current, although there are a few exceptions.

The term switching *Controller* implies that the switches are *External* to the IC. By using external PMOS and/or NMOS FETs, output currents up to about 40 A are possible.

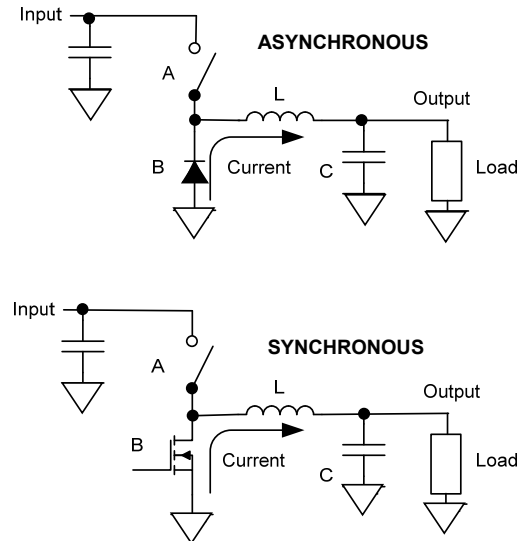
For higher currents, a parallel arrangement of buck converters, each operating with a phase offset. These types of converters are referred to as *Multiphase* controllers and can handle up to 40 A/phase.

The left side of the figure shows what is commonly referred to as an *Asynchronous* converter. A diode (usually a schottky diode) acts as the second switch. The diode is sometimes called a "freewheeling" diode or a "catch" diode.

The right side of the figure shows what is known as a *Synchronous* converter. In this case, both switches are active devices. The term "synchronous" implies that the switch drive signals must be carefully synchronized in order to ensure that both switches are not turned on at the same time, shorting the input to ground.

## Step-Down DC-to-DC Converters: Synchronous Rectification

- ◆ Switch B can be either a diode or a NMOS device because inductor current is going only in one direction.
- ◆ Switch B traditionally is a freewheeling, "catch" diode that turns on automatically when Switch A is turned off. (Asynchronous Operation)
- ◆ Many modern step-down converters have replaced the diode with a NMOS device (Synchronous Operation)
- ◆ **Advantages of Synchronous Rectification**
  - Higher efficiency at nominal load because  $I_{RMS}^2 \times R_{DS(ON)} < I_{RMS} \times V_D$
- ◆ **Disadvantages of Synchronous Rectification**
  - NMOS device can be more expensive than diode
  - Need for complementary drivers with anti-shoot through circuitry.
  - Efficiency is reduced at light loads because charge is removed from the output capacitor when the inductor current goes negative (This can be solved by adding a zero current crossing detector to disable the NMOS.)



We now look at synchronous rectification in more detail. Synchronous rectification has the chief advantage of higher efficiency because the diode is replaced with a low on-resistance NMOS device. The power dissipated in the NMOS device is generally less than that dissipated in the schottky diode for nominal output currents. As the duty cycle ( $V_{OUT}/V_{IN}$ ) decreases the gains in efficiency will increase in the synchronous rectification buck configuration. This is because the low-side B switch is "on" a higher percentage of the time for low duty cycles, and therefore its power dissipation becomes more significant. For high current loads, several NMOS FETs can be paralleled. At steady state operation current will be evenly shared because the NMOS gate-to-source temperature coefficient is positive. Catch diodes, on the other hand, should not be paralleled because their temperature coefficient is negative, and one of the diodes could start to carry the majority of the current causing thermal runaway.

Synchronous rectification requires careful timing in the two switch drive signals in order to ensure that both switches are not on simultaneously.

The efficiency of the synchronous rectifier is reduced at light loads because charge is removed from the output capacitor when the inductor current goes negative. This can be prevented by using a scheme that can change switch B to a unidirectional device at light output loads.

Care must be taken when the synchronous regulator is powered up that there is no voltage on the load (referred to as a *pre-biased load*). Otherwise the low-side switch will short the voltage to ground, unlike the simple diode low-side switch. Most modern synchronous regulators sense this pre-bias condition and disable the low-side switch until the output voltage reaches its nominal value.

## What Topology Depends Primarily on Output Current (Approximate Values Given Below)

### ◆ **<5A:**

- Asynchronous Controller (External Diode, External High Side Switch), ADP1864
- Synchronous Regulator (Internal High Side and Internal Low Side Switches), ADP2102, ADP2105, ADP2106, ADP2107, ADP2108

### ◆ **0.1A to 40A:**

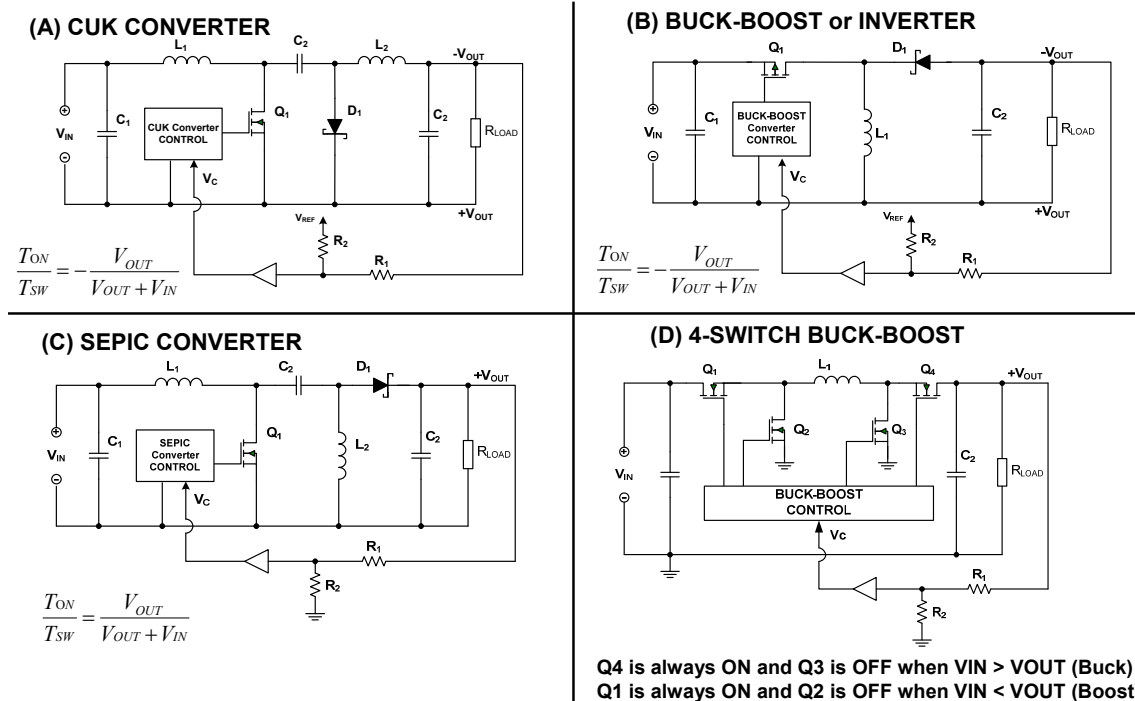
- Synchronous Controller (External High Side and External Low Side Switches), ADP1821, ADP1822, ADP1823, ADP1828, and ADP1829
- The ADP182x series have internal drivers capable of driving multiple N-channel MOSFETS in parallel. If the thermal environment allows for it, it is possible to get about 20A per pair, so the 40A is reached with a pair of MOSFETS on the high side and a pair on the low side.

These are some general guidelines showing where asynchronous and synchronous regulators and controllers are most often used.

For output currents less than 5 A, an asynchronous controller with an external diode and an external high-side switch, such as the ADP1864, is a good solution. For higher efficiency, synchronous regulators having internal high-side and low-side switches, such as the ADP2102, ADP2105, ADP2106, ADP2107, ADP2108 are good solutions.

For currents between approximately 0.1 A and 40 A, synchronous controllers with external switches, such as the ADP1821, ADP1822, ADP1823, ADP1828, and ADP1829, are good choices.

## Other Switching Topologies



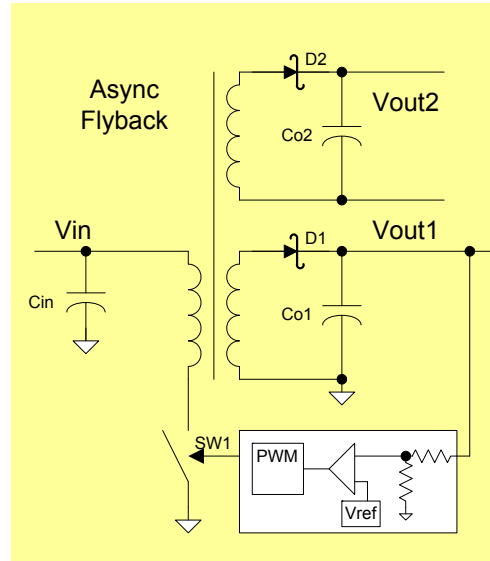
There are a variety of other switching converter topologies, and this figure shows a few of the more popular ones.

The CUK and Buck-Boost (Inverter) topologies shown in (A) and (B) provide a negative output voltage. The SEPIC and 4-Switch Buck-Boost shown in (C) and (D) provide a positive output voltage. The 4-switch Buck-Boost is an interesting topology, since it can step-up or step-down the input voltage and finds applications in battery operated devices. When the input voltage of the buck-boost is close to the output voltage, the converter runs in a 4-switch mode which allows a graceful transition between buck and boost modes. This feature can be extremely useful in battery powered systems.

The ADP2503 (0.6 A) and ADP2504 (1.0 A) are synchronous buck-boost regulators which have an input voltage range of 2.3 V to 5.5 V and outputs of 2.8 V, 3.3 V, 3.5 V, 4.2 V, 4.5 V, and 5 V. The 2.5 MHz switching frequency allows the use of a small 1  $\mu$ H ceramic inductor in an 0805 package. The devices use the basic topology of the 4-Switch Buck-Boost shown in (D) above.

## Isolated Topologies: Asynchronous Buck-Boost-Flyback

- ◆ **Multiple outputs track at fixed loading**
- ◆ **Most popular buck-boost**
- ◆  **$V_{OUT} > V_{IN}$  or  $V_{IN} > V_{OUT}$**
- ◆ **ADP1610, ADP1611, ADP1621**
- ◆ **Easy to isolate  $V_{OUT}$**
- ◆ **One magnetic element for multiple output voltages.**
- ◆ **Discontinuous Input Current**
- ◆ **Discontinuous Output Current**



There is an entire family of switching converter architectures which make use of transformers rather than a simple inductor. These are referred to as "isolated" topologies because of the electrical isolation provided by the transformer. These types of converters are generally more suitable system power supplies rather than simple POL applications. It is, however, worth mentioning a few of the most popular.

*Flyback* converters have been very popular in consumer equipment due to low cost, low parts count potential, and ease of isolation. At low output power, multiple outputs track reasonably well, but a low cost LDO is often used to improve regulation and reduce ripple. Noise in the form of switching spikes and ringing increases with output power, making this topology most useful for supplies which are 50 W or less.

The ADP1621 controller is well suited for this topology. The gate drive voltage on the ADP1621 is limited to 5 V, making it useful with FETs rated for 100 V or less. For a 1:n transformer (coupled inductor), the voltage applied across SW1 when the output diode is conducting is equal to  $V_{IN} + V_{OUT}/n$ . There is also ringing on this node due to parasitics in the transformer, PCB, and switch, so the voltage rating of the primary side switch needs to be approximately  $1.2 \times (V_{IN} + V_{OUT}/n)$  or higher, but not exceed 100 V.



## Key Specifications

- ◆ **Input Voltage Range:** Specifies the regulator input supply voltage range where all the regulator specifications are satisfied.
- ◆ **Output Voltage Accuracy:** Specifies the output voltage error due to line, load, process, and temperature variations. In some cases the accuracy is specified for a given input voltage and output current value. In this situation, we need to add the Line and Load variations in order to estimate the total regulator accuracy.
- ◆ **Load Regulation:** Is the circuit's ability to maintain the output voltage regulation under varying loading conditions.

$$LoadReg = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \text{ in (mV or V). Another form can be: } LoadReg(\%) = 100 \times \frac{\Delta V_{OUT}}{V_{OUT} \times \Delta I_{OUT}} \text{ in \% / A or \% / mA}$$

- ◆ **Line Regulation:** Is the circuit's ability to maintain the output voltage regulation under varying input supply voltage conditions.

$$LineReg = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \text{ in (mV or } \mu\text{V). Another form can be: } LineReg(\%) = 100 \times \frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}} \text{ in \% / V or \% / mV}$$

- ◆ **Dropout Voltage:** Is the minimum difference between unregulated input voltage and regulated output voltage for which the regulator operates within specification
- ◆ **Efficiency:** Specifies the power wasted by the regulator to perform input-output conversion

$$\eta(\%) = \frac{P_{OUT}}{P_{IN}} \times 100 \quad ; \quad P_{LOSS} = P_{IN} (1 - \eta)$$

The key regulator specifications are listed here for reference.

## Key Specifications (Continued)

- ◆ **Quiescent Current (Ground Current):** Is the biasing current for the regulation circuit, typically in  $\mu\text{A}$  range. This parameter is important in battery operated equipment since the quiescent current will be consumed even if the load is removed. In some cases a shutdown pin is available to disable completely the biasing circuit of the regulator ( $V_{\text{OUT}} = 0\text{V}$ ).
- ◆ **PSRR or Power Supply Rejection Ratio:** Is intimately related to the Line Regulation since the Operational (Error) Amplifier and regulator supply input are the same. The PSRR is expressed in dB and usually specified at specific frequency (PSRR deteriorate at higher frequency).

$$PSRR_{dB} = 20 \times \log_{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}}$$

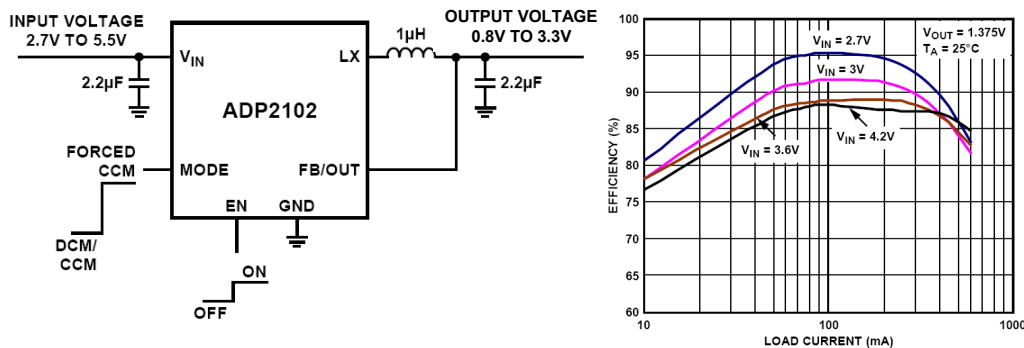
- ◆ **Output Noise:** This specification applies to Linear Regulators and quantifies the amount of noise generated by the internal circuits, most notably the Band Gap, it is specified in  $\mu\text{V rms}$  over a specific frequency range (typically 10Hz to 100kHz). Low-Noise Regulators provide a bypass filter pin for an external bypass capacitor.
- ◆ **Load Transient Response:** Specifies the regulator's ability to respond to rapid changes of the load current. In most cases the data sheet shows a waveform of the output voltage perturbation due to load current change. This information is useful to test the regulator's stability. Expressed as  $\Delta V_{\text{OUT}}$  for a  $\Delta I_{\text{OUT}}$  at a given  $di/dt$ .  $\Delta V_{\text{OUT}}$  will be a function of the converter bandwidth, Phase Margin, and power stage filter components.
- ◆ **Line Transient Response:** Similarly to Load Transient Response this parameter specifies the regulator ability to respond at rapid changes of the input voltage. Expressed as  $\Delta V_{\text{OUT}}$  for a  $\Delta V_{\text{IN}}$  at a given  $dV/dt$ .
- ◆ **Cross-Regulation:** In multi-regulator devices it is important to measure the influence of one regulator to another. For example in a dual regulator circuit the Cross-Regulation is specified as:

$$CrossReg = \frac{\Delta V_{\text{OUT1}}}{\Delta I_{\text{OUT2}}} \quad \text{or} \quad \frac{\Delta V_{\text{OUT2}}}{\Delta I_{\text{OUT1}}}$$

This is a continuation of key specifications.

## Switching Frequency Considerations

- ◆ Early switchers operated in the 20kHz to 100kHz region
- ◆ Higher frequencies allow smaller inductors, but produce larger switching losses
- ◆ Modern switchers operate in the 100kHz to 3MHz range
- ◆ Frequency of some switchers can be "dithered" (spread spectrum) to reduce EMI/RFI
- ◆ Frequencies of some switchers can be synchronized to avoid beat frequency interaction
- ◆ ADP2102 3MHz synchronous switching regulator uses 1 $\mu$ H inductor with 95% efficiency for a 2.7V input and a 1.375V output @ 200mA



Early switchers operated in the 20 kHz to 100 kHz range, but there are several reasons for increasing the switching frequency. Higher frequencies allow smaller inductors and decrease size and parts cost. However, higher switching frequencies generate more switching loss and therefore require faster switches in order to maintain high efficiency.

In some applications where EMI/RFI is a major concern, it is possible to "dither" the switching frequency and reduce EMI/RFI. This is done by intentionally varying the switching frequency so that the switching energy is spread over a band of frequencies, thereby reducing the energy contained at any single frequency.

Some switchers can have their switching frequency synchronized to other switchers.

The ADP2102 switching regulator (internal switches) operates at 3 MHz and yields 95% efficiency for a 2.7 V input and a 1.375 V output at a 200 mA using a 1  $\mu$ H ceramic inductor in an 0805 package. Ceramic inductors are smaller and cheaper than winding coils, and typically half price. Minimum required input and output capacitors are 2.2  $\mu$ F ceramics with X5R or X7R dielectrics.

The ADP2108 switching regulator also operates at 3 MHz and can supply up to 600 mA. Input voltage range is 2.3 V to 5.5 V. Fixed output voltage options are available from 1.0 V to 3.3 V.

## Methods for Designing Switchers

### ◆ The Traditional Way:

- Use equations on the data sheet and a hand calculator (more than 50 equations are sometimes required (all of which will probably ignore non-linearities))
- Design a spreadsheet to solve the equations
- Ridley's Excel-Based "POWER 4-5-6"
- These methods assume an experienced power designer

### ◆ The Easier Way:

- Use manufacturer's website design tool (ADIsimPower) for straightforward POL applications
- Use manufacturer's FAE support organization for complex designs

### ◆ Based on design requirements, a good design tool should yield:

- An optimized design that "barely" meets the dc and ac specifications and is not an "overdesign"
- Complete schematic
- Top-level electrical, stability, and thermal analysis
- Reasonable "What if" capability
- Bill of materials, including manufacturers' part numbers
- Evaluation boards for prototyping

The textbook approach to design a switching converter can be a daunting task for the engineer who must quickly design a point-of-load supply on a PC board. Most IC switching converter data sheets supply the large number of required equations, but solving them can easily get out of hand even using a spreadsheet.

Fortunately most successful manufacturers of switching converter ICs provide user-friendly selection guides and interactive website design tools for straightforward POL applications. An experienced field applications engineering support group should be available to assist with more complex designs.

Rapid design turnaround times are usually required because history tells us that the power supply portion of the PC board is usually the last thing to be designed.

There are several requirements of a good design tool. First and foremost, the design should be optimized to meet the required specifications, but should not be an "overkill." It should "barely" meet the dc and ac performance objectives.

The tool should yield a complete schematic, a top-level electrical, stability, and thermal analysis. In addition a complete bill of materials including manufacturer's part numbers is needed.

The tool should also provide some capability in playing "what if" scenarios, such as optimizing for efficiency, parts count, parts cost, or real estate.

Evaluation boards should be available for prototyping the final design. Custom evaluation boards for qualified opportunities should be available within one week.

Analog Devices' ADIsimPower design tool is discussed later in this section, and meets the requirements specified above.

## Fundamental Switcher Calculations: This is Only the Beginning!

- ◆ **Select the Inductor Current Ripple,  $\Delta I_L$  (Peak-to-Peak)**
  - Typically 30% to 40% of the nominal load current.
  - Increased inductor ripple current improves transient response and can decrease physical size.
  - Increased inductor ripple also increases output voltage ripple, RMS currents through inductor and switches, and inductor core loss.
- ◆ **Calculate the Inductor Value Based on Ripple Current,  $T_{ON}$ , and  $T_{OFF}$** 
  - $L = T_{ON} \times V_{ON} / \Delta I_L = T_{OFF} \times V_{OFF} / \Delta I_L$
  - Through the principle of Volt-second balance one can equate the target inductance value through either the off-time or on-time equation.
- ◆ **Calculate the Output Voltage Ripple Based on:**
  - Inductor Ripple Current
  - Bulk Capacitor Value
  - Bulk Capacitor ESR

Continued.....

This shows a few of the beginning steps in a switching converter design. Most switching converter data sheets provide these design steps along with the appropriate equations.

## Stability and Transient Considerations

- ◆ **A switching regulator/controller is a closed-loop feedback system and is analyzed using basic control loop theory.**
- ◆ **There are excellent tutorials, equations, and graphs on the data sheet which provide the procedure for stabilizing the loop and optimizing load transient response.**
- ◆ **Stability/transient analysis depends on control mode architecture:**
  - Voltage control mode
  - Current control mode
- ◆ **PWM (Pulse Width Modulation)**
  - Constant frequency
- ◆ **PSM (Power Saving Mode) for efficiency for light loads**
- ◆ **PFM (Pulse Frequency Modulation)**
  - Constant ON time
  - Constant OFF time
- ◆ **The total output voltage deviation upon a large high di/dt load step is primarily dependent on the regulator's large signal behavior, which is not characterized by the control loop.**

Continued.....

Since a switching converter is a closed-loop feedback system, it must be analyzed for stability and transient response using basic control loop theory. This aspect of switching converter design can become especially tedious to the engineer unfamiliar with switching supplies.

Stability and transient analysis depend on the control architecture: voltage mode, or current mode.

Again, the data sheets provide guidelines in the design, but there is an easier way!

## Power Losses in Switching Supplies Determine Efficiency

◆ **Efficiency Depends on the Total Power Loss in the Components:**

- Regulator/Controller IC Power Loss
- Inductor Power Loss (conduction and core loss)
- Input and Output Bulk Capacitor Power Loss (due to ESR)
- Diode Power Loss (Asynchronous)
- MOSFET Switching Power Loss
- MOSFET Conduction Losses
- Sense Resistor Power Loss
- Feedback Resistor Network Power Loss
- Efficiency Equations:

$$\eta = \frac{P_{IN} - P_{LOSS}}{P_{IN}} \quad P_{LOSS} = P_{IN}(1 - \eta) \quad \eta(\%) = \frac{P_{OUT}}{P_{IN}} \times 100$$

◆ **Thermal Analysis**

Continued.....

It is important to calculate the power loss in the various elements in the switching converter. This not only allows efficiency to be calculated but provides the necessary information to perform a thermal analysis.

Calculating each of these loss elements can be relatively easy ( $P = I \times V$ ) or extremely difficult. MOSFET switching loss, for example, is a number that is not incredibly difficult to approximate. However, if all non-linearities are taken into account, one could spend a considerable amount of time arriving at an answer. Fortunately, the parasitics that cause switching loss can be approximated to arrive at results that are close enough.

ADIsimPower is Analog Devices' new dc-to-dc converter power management tool. This tool is available on the ADI website. The user provides power supply parameters, and ADIsimPower provides a solution selection guide that offers a list of topologies, ICs, and performance estimates. From this information, the designer can then proceed to the next step of the tool where he will get a customized schematic, BOM, and performance specs optimized to the design criteria.

ADIsimPower requires no login and no registration. The tool is created by experienced power supply designers. You can find a link to ADIsimPower under the Design Tools link on [www.analog.com](http://www.analog.com).

Before discussing ADIsimPower in detail, we will examine a few typical examples of POL power applications.

## Powering FPGAs



## FPGA Power Supply Considerations

- ◆ **Variable requirements between manufacturers and within part families**
  - Xilinx: *Spartan™* II, IIE, 3; *Virtex™* II, II Pro, II Pro X, 4, 5
  - Altera: *Cyclone™* II, III; *Stratix®* II, IIGX III, IIIL, IIIE, IIIGX, *Aria* GX
- ◆ **Multiple Voltage Rails Required: Core, Auxiliary, I/O, Transceivers, etc.**
- ◆ **Core Voltage (Typically 1.2V for 90nm processes, 0.9V for 65nm)**
  - Monotonic Ramp-Up required for proper initialization sequence.
  - Tolerance of 50mV or 60mV (5%) includes steady state, ripple, and load transient.
- ◆ **Core Current must be calculated based on design: 1A to 10A typical,**
  - But designer should allow adequate margin for error and software changes which can affect dynamic current.
- ◆ **High speed I/O transceivers generally require low noise linear regulators.**
- ◆ **External SDRAM Voltage Requirement: 1.8V (2.5V older SDRAMs).**
- ◆ **Power supply sequencing may be needed, but requirements vary.**

Field programmable gate arrays (FPGAs) are critical building blocks in many system designs. Manufacturers of FPGAs, such as Altera, Xilinx, and others, provide extensive documentation and on-line assistance in selecting, programming, and calculating the power requirements for these devices.

Each manufacturer offers several product families of FPGAs, each family offering varying degrees of performance, processing capability, and size. Simply selecting the appropriate device for a given application can be a daunting task.

After selecting the FPGA, calculating the current requirements and power dissipation based on the number of active tiles and other parameters is a critical step. Here again, the manufacturers also offer various tools to assist in the task.

FPGAs almost always require dedicated POL supplies. At a minimum, the FPGA will require a separate I/O voltage and a core voltage. Other auxiliary voltages may also be needed, as well as low noise supplies for the high-speed I/O section, if using such a device.

There is generally a fairly tight requirement on the supply voltage, typically  $\pm 5\%$ . This implies  $\pm 60$  mV for a 1.2 V core voltage. The  $\pm 5\%$  specification includes transient response to load steps as well as dc tolerance and ripple voltage.

There is also a requirement that the supply voltage ramp-up monotonically in a defined period of time to ensure proper internal initialization. In some cases, the voltages must be applied in a specific sequence.

## Proper Application of Power to FPGA

- ◆ A certain sequence of events happens within the FPGA as the core voltage is applied (power-on reset, memory and timing initialization, etc.)
- ◆ Must reach core voltage monotonically between  $T_{MIN}$  and  $T_{MAX}$  to ensure proper initialization. It is mandatory that the POL regulator has a soft-start feature in order to control this ramp-up.
- ◆ Ramp rates also specified for other voltages:  $V_{CCAUX}$ ,  $V_{CCO}$
- ◆ Too little bulk capacitance makes load transient too large.
- ◆ Too much bulk output capacitance reduces load transient but increases charging current requirement.
- ◆ Increasing bulk capacitance beyond a certain point will force regulator into current limit and possibly cause a non-monotonic condition.

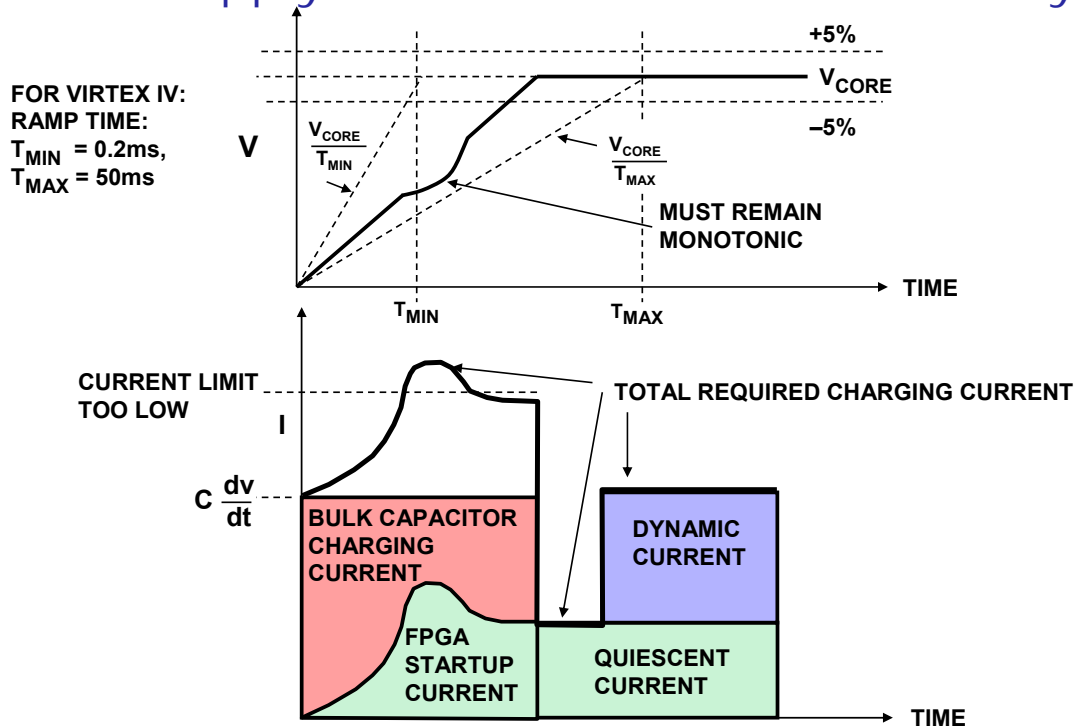
A certain sequence of events internal to the FPGA must occur during power-up in order for proper initialization and operation of the device. This includes power-on reset, memory, and timing initialization, etc.

For proper initialization, the core voltage must ramp-up to its final value monotonically within a specified time interval between  $T_{MIN}$  and  $T_{MAX}$ . The same ramp rate requirement generally applies to the other voltages as well. A POL regulator with a soft-start feature is mandatory in these applications.

In order to minimize transients due to rapid load step current changes, the total bulk capacitance on the POL regulator output can be quite large. However, the regulator must charge the bulk capacitor at a specified ramp rate,  $dv/dt$ , which implies a minimum charging current,  $I = C dv/dt$ . In addition, the regulator must supply the start-up current to the FPGA. If the regulator goes into current limit, its output will cease to be monotonic, and the FPGA may not initialize properly.

The bulk capacitor should therefore be large enough for proper load step transient response, but not so large that the POL regulator current limits and is non-monotonic.

## Power Supply Must Charge Bulk Capacitance and Supply Inrush Current Monotonically



This is a good example of where too much bulk capacitance can hurt.

The voltage ramp-up must be completed within a specified time, in this case, 50 ms. The regulator must charge the bulk capacitance with a current of  $I = C \frac{dv}{dt}$ . In addition, the regulator must supply the FPGA start up current. The capacitor charging current and the FPGA start-up current must not exceed the current limit of the POL regulator, or a "dip" in the output voltage can occur, causing non-monotonicity.

In the figure above, the current limit of the POL regulator is too low, and the start-up voltage ramp has a corresponding "dip" which could cause initialization problems.

As previously mentioned, the soft-start feature of the POL regulator can be used to control the ramp rate, but care must be taken in selecting the value for the total bulk capacitance in order to ensure that both load transient performance and monotonic ramp-up can be achieved simultaneously.

## Sequencing/Power-On Issues with FPGAs

- ◆ Most FPGAs do not have "strict" sequencing requirements
- ◆ However, some FPGAs have "recommended" sequencing that will minimize inrush current at power-on
- ◆ Maximum required "Start-Up or Power-On" current is usually specified by FPGA manufacturer.
- ◆ The "power-on" current does not include the extra current required to charge the bulk capacitance at the specified ramp rate
- ◆ In most cases, sequencing is not required if supplies can meet the power-on current requirements, and the supplies are brought up more or less simultaneously.
- ◆ As with all CMOS logic, the digital input voltages to the FPGA should not be more than 0.3V to 0.5V above the I/O power supply during startup.
- ◆ The external FPGA clock oscillator must be running during the start-up sequence for proper initialization.
- ◆ Always read the FPGA data sheet and user manual.

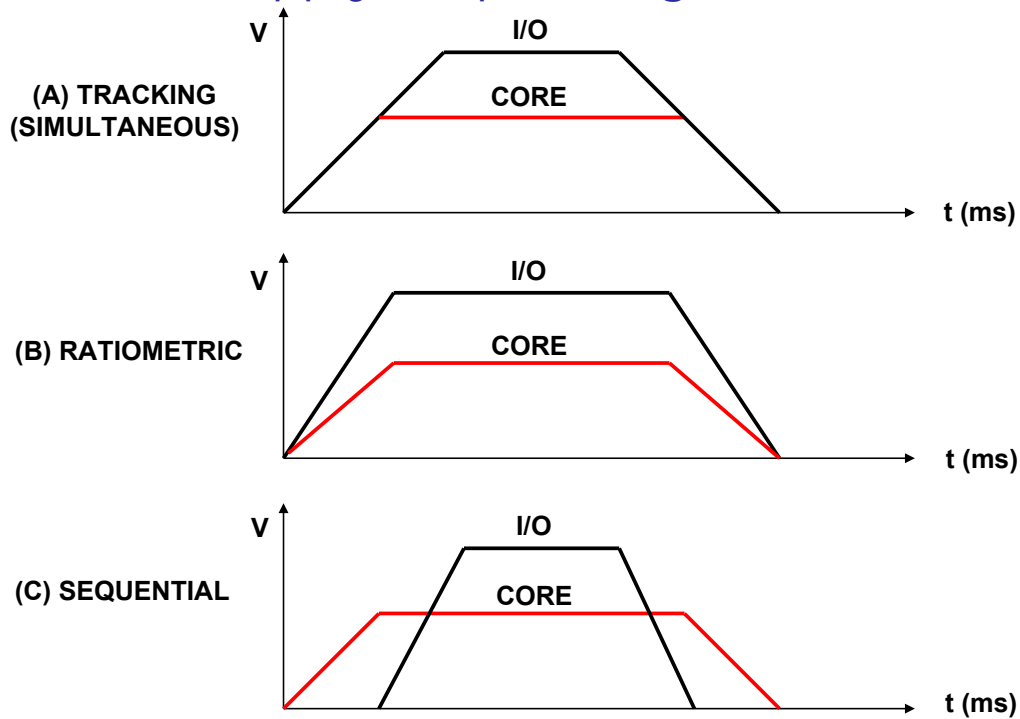
Most FPGAs do not have specific sequencing requirements. However, it may be desirable to sequence the supplies in order to prevent large inrush current, and many FPGAs have a recommended sequence if the supplies are not turned on simultaneously.

However, there is usually no need for sequencing if the supplies can meet the inrush current requirements and maintain a monotonic ramp.

As with all CMOS logic, the digital input voltages to the FPGA should not be more than 0.3 V to 0.5 V above the I/O power supply during startup.

The FPGA data sheet should be consulted with respect to the external clock oscillator requirements. In most cases, the oscillator must be running during the ramp-up sequence for proper initialization.

## Simultaneous, Ratiometric, and Sequential Supply Sequencing Methods



This shows the three common methods of sequencing the core and I/O voltages.

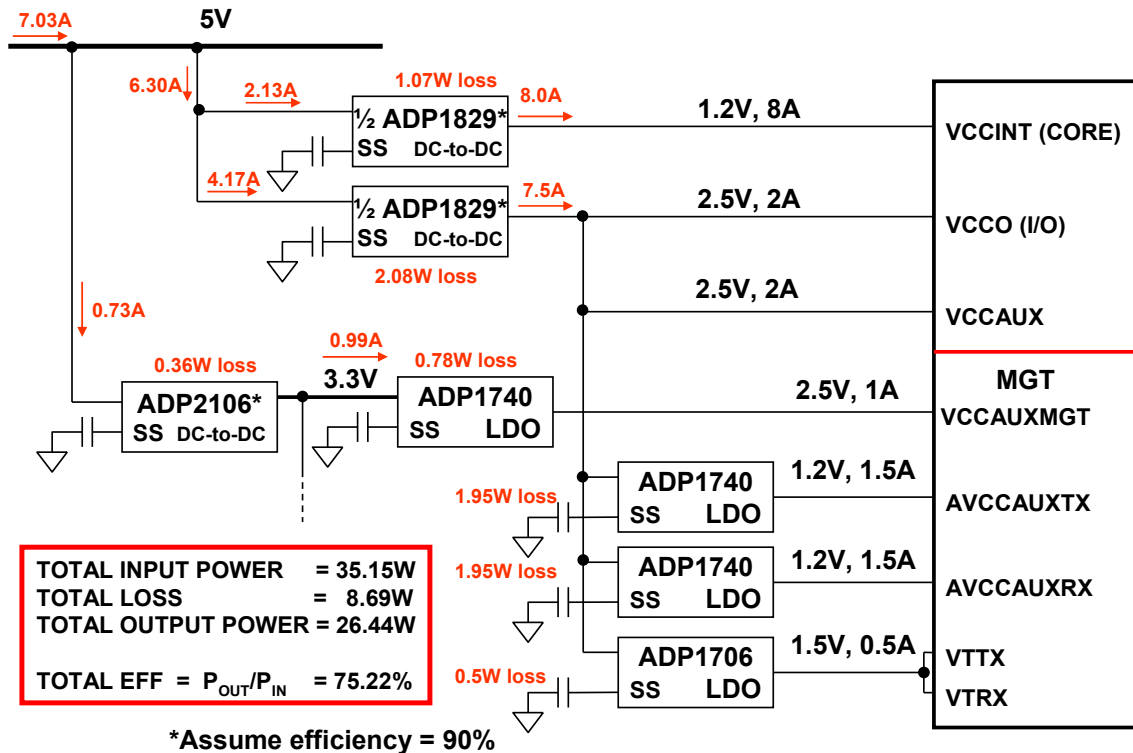
The *Simultaneous* method is shown in (A), where the core and I/O voltages track each other during power-on.

The *Ratiometric* method of sequencing is shown in (B).

The *Sequential* method shown in (C) is often used to prevent large inrush currents.

Sequencing is most easily accomplished with ICs designed specifically for the task and is described in more detail in Section 2 of the seminar.

## Xilinx Virtex-4 FPGA Power Supplies



This shows a possible arrangement for supplying power to the Virtex-4 FPGA from a single 5 V bus.

The values of current chosen in the example are representative. An actual FPGA design may have different values and therefore a different power structure could be required.

The core voltage of 1.2 V and the 2.5 V I/O and auxiliary voltage are supplied by a dual synchronous switching controller, the ADP1829. The ADP1829 phase shifts the switching of the two step-down converters by 180°, thereby reducing the input ripple current. This reduces the size and cost of the input capacitors.

The 2.5 V output of the ADP1829 also acts as an intermediate bus to supply the low noise LDOs required to drive the MGT portion of the FPGA. The soft-start feature of the various regulators and controllers can be used to control the slope of the ramp during power up. Finally, an ADP2106 synchronous switching regulator generates an intermediate 3.3 V bus which drives an ADP1740 LDO which in turn generates the auxiliary 2.5 V for the MGT section.

The 3.3 V can be distributed to other parts of the system if desired.

Note that the diagram does not show the important localized decoupling at each of the power supply pins of the FPGA.

## Switching Supply Error Budget Must Include Transient in Most FPGA Applications

**Total Error Budget (Including Load Transient)  
for 1.2V Core Voltage =  $\pm 5\%$  ( $\pm 60\text{mV}$ )**

ERRORS	CALCULATION	%
$V_{\text{REF}}: \pm 1.0\%$	1.0%	1.00
1% FEEDBACK RESISTORS	WORST CASE = 1%	1.00
OUTPUT RIPPLE	1% OF $V_{\text{OUT}}$ (p-p)	0.50
LINE REG: 0.12mV/V	$0.12\text{mV/V} \times 5\text{V} \times 5\%$	0.03
LOAD REG: 0.07%/A	$0.07\%/A \times 10\text{A}$	0.70
TOTAL STATIC ERRORS		3.23
LOAD TRANSIENT ERROR	$\{(5\% - 3.23\%) \div 100\} \times 1.2\text{V}$	21.2mV

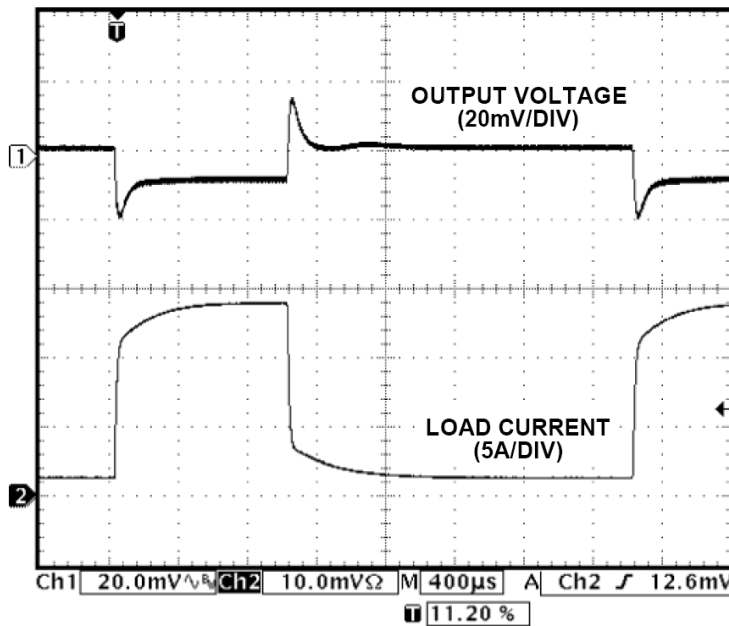
**DATA BASED ON ADP1829 SWITCHING CONTROLLER**

The power supply error budget for an FPGA must not only include the static errors but also the load transient error resulting from the load step.

This table shows how the various error sources are allocated for a typical application using the ADP1829 dual synchronous switching controller.

The basis core voltage of 1.2 V has a total tolerance of  $\pm 5\%$  ( $\pm 60\text{ mV}$ ). The total static errors include the following: internal voltage reference error, feedback resistor tolerance, output voltage ripple, line regulation, and load regulation. The sum of the static errors is 3.23%. This leaves  $5\% - 3.23\% = 1.77\%$ , or 21.2 mV for the transient error.

## ADP1829 Load Transient Response



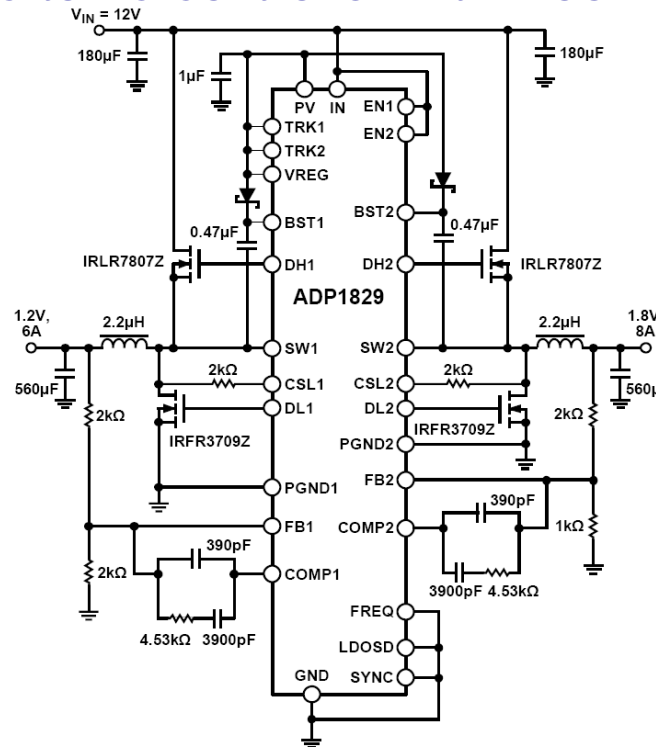
**1.5A TO 15A LOAD TRANSIENT, 12V INPUT**

The ADP1829 load transient response is shown here for a load current step of 1.5 A to 15 A. Note that the total output transient is approximately 38 mV p-p.

It should be noted that achieving this level of transient performance often involves some level of in-circuit optimization as well as a good design tool (ADIsimPower).



## ADP1829 Dual, Interleaved, Step-Down DC-to-DC Controller with Tracking



The ADP1829 is a versatile, dual, interleaved, synchronous PWM buck controller that generates two independent output rails from an input of 3.0 V to 18 V, with power input voltage ranging from 1.0 V to 24 V. Each controller can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators. The two channels operate 180° out of phase, reducing stress on the input capacitor and allowing smaller, low cost components.

The ADP1829 is ideal for a wide range of high power applications, such as DSP and processor core I/O power, and general-purpose power in telecommunications, medical imaging, PC, gaming, and industrial applications. The ADP1829 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost.

For noise-sensitive applications, it can also be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1 MHz. The ADP1829 includes soft start protection to prevent inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET sensing.

For applications requiring power supply sequencing, the ADP1829 also provides tracking inputs that allow the output voltages to track during startup, shutdown, and faults. This feature can also be used to implement DDR memory bus termination.

The ADP1829 is specified over the -40°C to +125°C junction temperature range and is available in a 32-lead LFCSP package.

Interleaving the switching of the two step-down converters by 180° reduces the input ripple current. This reduces the size and cost of the input capacitors.

# Powering DSPs

[www.analog.com/dsp](http://www.analog.com/dsp)

## Typical Low Power DSP and FPGA Voltage and Current Requirements

	PART NUMBER	V <sub>CORE</sub> (V)	V <sub>I/O</sub> (V)	I <sub>CORE</sub> (mA)	I <sub>I/O</sub> (mA)
<b>ADI</b>	<b>ADSP-21xx (16-bit)</b>	<b>1.8 to 2.5</b>	<b>3.3</b>	<b>25 to 200</b>	<b>15</b>
	<b>ADSP-BF531, ADSP-BF532, ADSP-BF533</b>	<b>0.8 to 1.4</b>	<b>2.5 to 3.3</b>	<b>25 to 300</b>	<b>150</b>
	<b>ADSP-BF534, ADSP-BF536, ADSP-BF537</b>	<b>0.8 to 1.2</b>	<b>2.5 to 3.3</b>	<b>25 to 300</b>	<b>150</b>
	<b>ADSP-21xxx (SHARC)</b>	<b>1.2 to 3.3</b>	<b>3.3</b>	<b>940 (typ)</b>	<b>72</b>
<b>Marvell</b>	<b>PXA270 (Intel)</b>	<b>0.8 to 2.0</b>	<b>1.5 to 3.4</b>	<b>600 (typ)</b>	<b>150</b>
<b>Xilinx</b>	<b>Spartan IIE FPGA XC2S50E, XC2S300E</b>	<b>1.8</b>	<b>1.5 to 3.3</b>	<b>200 to 2000</b>	<b>500</b>
<b>Altera</b>	<b>Max II CPLDs</b>	<b>1.8 to 3.3</b>	<b>1.5 to 3.3</b>	<b>100 to 400</b>	<b>150 to 400</b>
	<b>Cyclone FPGA</b>	<b>1.5</b>	<b>1.5 to 3.3</b>	<b>1000 (typ)</b>	<b>600</b>

**NOTE:** Approximate currents only. Actual currents depend on operating conditions.

DSPs are optimized for performing fast arithmetical operations. A repetitive series of multiplications and accumulations forms the basis of digital filters and FFT processing, and DSPs perform these functions much faster and more efficiently than standard microprocessors.

Field programmable logic gate arrays (FPGAs) and complex programmable logic devices (CPLDs) can also be programmed to perform these and other functions.

This table lists some popular relatively low power processors suitable for general purpose applications, along with the core and I/O typical voltages and currents.

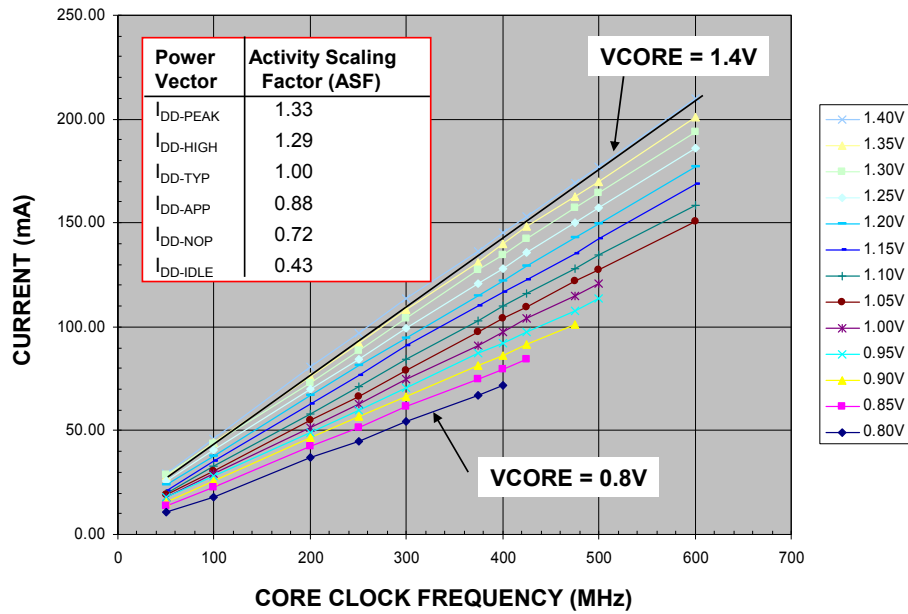
It should be noted that the actual core and I/O currents (to a lesser degree) are highly dependent on the task activity, core voltage, clock frequency, process, and temperature.

These devices all have current requirements less than 2 A, which makes them ideal candidates for integrated synchronous switching regulators.

Because of their widespread usage in portable applications, efficiency, parts cost, and total size are important parameters of the POL design.

In the following section we examine the DSP core current variation and offer some easy solutions to core and I/O voltage supplies.

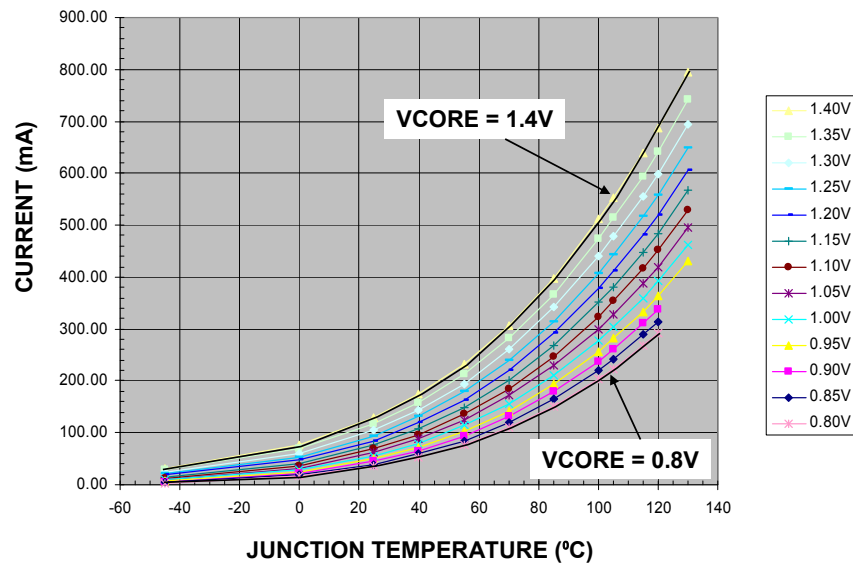
## ADSP-BF534, ADSP-BF536, ADSP-BF537 $I_{DD}$ Typical Dynamic Current ( $I_{DD-BASELINE-DYN}$ )



DSP dynamic operating current is highly dependent on the core voltage and the processor clock frequency as shown in this figure for the ADSP-BF534, ADSP-BF536, and ADSP-BF537 family of processors. This allows the core voltage and clock frequency to be optimized for a specific task.

This is a "baseline" current and can be viewed as being scaled by the type of instructions being executed in the processor. There is a table in the figure that gives some representative activity scaling factors. The peak value is a worst case with dual multiply-accumulates (MACs), and is not sustainable—a real application would be a mix of activities, and would typically correspond to a 1.0 multiplier. For low to idle activity, the current consumption drops about in half of the baseline value.

## ADSP-BF534, ADSP-BF536, ADSP-BF537 Maximum Static Current ( $I_{DD-DEEP\ SLEEP}$ )



One issue that should definitely be considered is the relatively high leakage currents of some of the latest high speed CMOS processes, (i.e the 0.13  $\mu\text{m}$  "fast" process used for the ADSP-BF537). The graph in the figure shows the "deep sleep" maximum static current as a function of junction temperature for various core voltages. Also, part-to-part variations in the process can have  $> 50\text{ mA}$  variation in current while in the "sleep" mode. As we target faster frequencies, a price is paid with higher leakage currents and wider variations in the process parameters. ADI is introducing an "LP" version of the Blackfin® ADSP-BF52x parts which will be on a slower process and limited to lower operating frequencies (300 MHz to 350 MHz core). In addition, DSPs with large internal memories can have significant leakage when in the "sleep" modes.

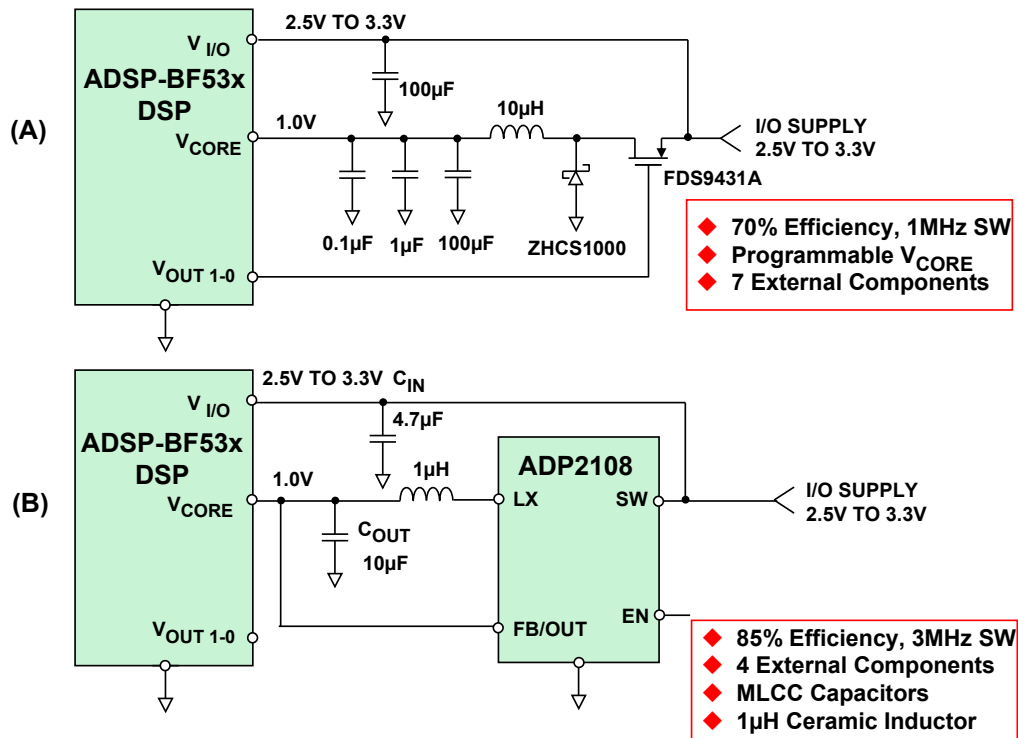
And another very significant issue is the relationship of static current to temperature. This again is primarily due to the high leakage currents of fast processes, and can lead to a  $5\times$  increase in current as temperature goes from 20°C to 100°C—and it is more of an exponential relationship (and also increases with core voltage). Therefore, the "static" leakage can be as high as the "dynamic" current.

A good guideline is a 1:4 ratio of "low" load to "high" load for the processors, and for the ADSP-BF537, this would approximately be 80 mA to 320 mA.

### REFERENCE:

"Estimating Power for ADSP-BF534/BF536/BF537 Blackfin Processors," *Engineer-to-Engineer Note EE-297*, 2007, Analog Devices, [www.analog.com](http://www.analog.com)

## Blackfin Power Solutions



Most of the Blackfin DSPs have an on-chip 1 MHz switching controller as shown in (A). The core voltage is derived from the I/O voltage. This circuit requires an external PMOS high-side switch and a free-wheeling Schottky diode as well as input and output filter capacitors. The core voltage can be programmed in 50 mV increments, and the efficiency is approximately 70%.

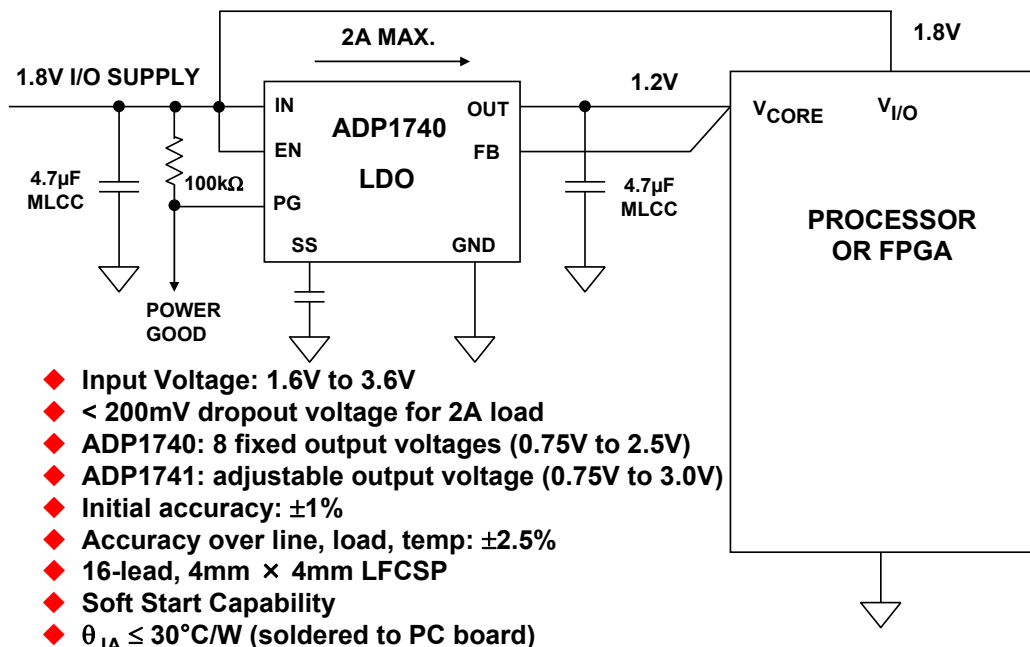
The ADP2108 600 mA 3 MHz synchronous switching regulator makes an attractive alternative to the internal regulator. The design is shown in (B). Only 4 external components are required (including the ADP2108), and the efficiency is greater than 80% for a 600 mA load current. It's input voltage range is 2.3 V to 5.5 V. In this application, it is driven by the I/O supply which must be between 2.5 V and 3.3 V for the BF53x series. A small 1 µH ceramic inductor and two MLCC capacitors are the only passive components required in the design. The design shown in (B) was done using ADIsimPower.

Most DSPs are relatively immune to power supply sequencing issues. They are usually initialized through an external non-volatile RAM, and an external supervisory circuit should always be used to reset the DSP on power-up. The DSP data sheet should be carefully checked for clock requirements on power-up. Some DSPs require that the clock be present during the initial power-on reset time. Regardless, the data sheet must always be consulted regarding these issues.

### REFERENCES:

1. "Switching Regulator Design Considerations for ADSP-BF533 Blackfin Processors," *Engineer-to-Engineer Note, EE-228*, Analog Devices, 2005, [www.analog.com](http://www.analog.com).
2. "Using External Switching Regulators with Blackfin Processors," *Engineer-to-Engineer Note, EE-339*, Analog Devices, 2008, [www.analog.com](http://www.analog.com).

## A Simple Solution to a Tricky Problem: Replacing 1.8V Core Supply with 1.2V Supply



Processors are rapidly moving to faster CMOS processes which have correspondingly lower geometries and hence lower core voltage requirements. For instance, upgrading from a 1.8 V to a 1.2 V core voltage is a common problem. Rather than redesign the switching supply, an attractive alternative can be the use of a simple LDO as shown in this figure.

The ADP1740 LDO has only 200 mV dropout voltage for a 2 A load. In the example shown it is used to regulate the 1.8 V I/O supply down to 1.2 V. The power that must be dissipated in the ADP1740 is therefore  $2 \text{ A} \times 0.6 \text{ V} = 1.2 \text{ W}$ . The ADP1740 16-lead, 4 mm  $\times$  4 mm LFCSP package with an exposed pad has a thermal resistance of  $\theta_{JA} = 30^\circ\text{C/W}$ , therefore the junction-to-ambient temperature rise is only  $1.2 \text{ W} \times 30^\circ\text{C/W} = 36^\circ\text{C}$ .

The ADP1740 is designed to operate with  $V_{IN}$  as low as 1.6 V to increase efficiency. The low 200 mV nominal dropout voltage at a 2 A load improves efficiency and allows operation over a wider input voltage range. In the above example, the efficiency is  $1.2 \div 1.8$ , or 67%.

The ADP1740 optimizes powering of core voltages between 0.13  $\mu\text{m}$  to 65 nanometer process geometries directly from the I/O voltage. This minimizes complexity by reducing component count and ensures proper supply voltage sequencing protecting the system IC device load.

The ADP1740 has an internal soft start that provides a constant startup time of 200  $\mu\text{s}$ . Short circuit protection and thermal overload protection protect the devices in adverse conditions.

A power good output allows power system monitors to digitally check the health of the output power rail voltage.

For lower core currents, the ADP170, 300 mA LDO operates on input voltages between 1.6 V and 3.6 V. Output voltage options from 0.8 V to 3.0 V are available.

For I/O voltages less than 1.6 V, the ADP130 dual, 350 mA LDO operates with input voltages between 1.2 V and 3.3 V. The device requires an additional bias voltage of 2.3 V to 5.5 V.

# ADIsimPower

[www.analog.com/adisimpower](http://www.analog.com/adisimpower)



## What is ADIsimPower?

- ◆ **Web based DC-to-DC power management tool available to anyone with an internet connection**
- ◆ **Includes integrated “solution” selection guide**
- ◆ **Produces a Schematic, BOM, and performance specs customized for *your* application**
- ◆ **Requires no registration and no login**
- ◆ **Architected, designed, and used by Power Management Application Engineers**
- ◆ **Where do I find it?**



ADIsimPower is Analog Devices' new dc-to-dc converter power management design tool. This tool is available on the ADI website. The user provides power supply parameters, and ADIsimPower provides a solution selection guide that offers a list of topologies, ICs, and performance estimates. From this information, the designer can then proceed to the next step of the tool where he will get a customized schematic, BOM, and performance specs optimized to the design criteria.

ADIsimPower requires no login and no registration. The tool is created by experienced power supply designers. You can find a link to ADIsimPower under the Design Tools link on [www.analog.com](http://www.analog.com), or simply go to [www.analog.com/adisimpower](http://www.analog.com/adisimpower).

## ADIsimPower Value Advantages

- ◆ **Differentiators**
  - **Intelligent Selector Guide that predicts performance in the four major design goals to rank available solutions**
  - **User chooses the primary design goal: Cost, Size, Efficiency, or Parts Count**
  - **Pre-qualified components library includes unpublished data**
  - **Comparative 1k pricing given on all components**
  - **Input filter support for crosstalk suppression**
  - **Designs for load transient steps from 10% to 100% of maximum output current**
  - **Dissimilar output capacitors are used to achieve large and small signal targets**
  - **Prototyping PCBs sold for fast verification**
- ◆ **ADIsimPower is NOT a Simulation Program**
  - **Competitors offer simulation in place of custom design support**
  - **Users must use a simulator and hours of design time trying to tweak a data sheet circuit to meet requirements**

ADIsimPower is not a copy of any other design tool. It mimics the process a power engineer would use to design a converter. It has several features that distinguish it from competitors' tools.

The selector guide in View 2 is not a parametric IC search. It is a solution selector guide that estimates and compares performance of multiple converters and topologies. Many competitors' tools will provide you with a list of ICs that will work, but they do not qualify and quantify how they might perform in relation to each other.

ADIsimPower users can select their primary design goal based on their application.

The customized BOM has a list of components that are qualified and optimized to work in the configuration provided by the user. The qualification process uses data that is both published and unpublished. Analog Devices has worked with the manufacturers of the various components in the converter to get 1k pricing to allow the user make price versus performance tradeoff decisions.

ADIsimPower also has an option that will design an optimized input filter to suppress crosstalk if necessary.

The tool will design the output filter to meet load transient and output voltage ripple specifications by using dissimilar output capacitors, a feature which is not offered in competitors' design tools.

Once the user is satisfied with the design ADIsimPower has provided, he is given the means to build and test his design by ordering a blank PCB that will accommodate the design.

ADIsimPower is not a time-based simulation design tool. While simulation tools can be very useful, they generally require expertise in power electronics that most designers do not have.

## Vendor Database

- ◆ **Total Number of Parts in Database Exceeds 4000**
  - All have behaviors that are unique to their construction that are modeled by working with their MFGs to get unpublished data.
- ◆ **Capacitors – MLCC, Tantalum, Aluminum Organic, Aluminum Electrolytic, and more...**
  - Performance predicted for:
    - ◆ DC Voltage Applied
    - ◆ Temperature
    - ◆ ESR over Frequency
- ◆ **Inductors – Ferrite, Powdered Iron, Hybrid Materials**
  - Range of applications: Mobile, VRM, Isolated
  - Core loss data obtained directly from manufacturer
  - Coilcraft parts included
- ◆ **MOSFETs and Diodes – Parts optimized for cost, efficiency, and size included in database**
  - Vendors
    - ◆ NEC, Infineon, Vishay, IR, ON, Diodes Inc
  - DC and transition losses predicted for:
    - ◆ Drive Voltage
    - ◆ Temperature
    - ◆ Vds Voltage Applied

The vendor database consists of the following parts:

### Inductors

Materials matter when determining which is the best part. The unique properties of each of these materials has been taken into account via the core loss equations. Much of this data is not published by the manufacturer.

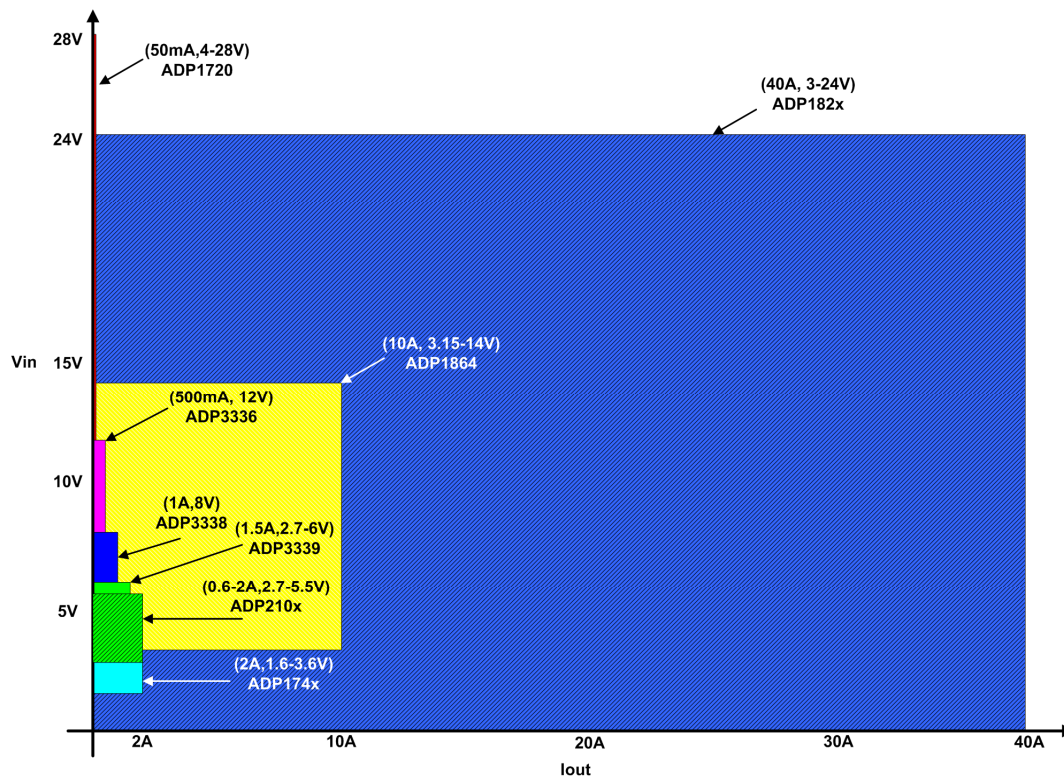
### Capacitors

Many types are included in database. Each have different behavior over temperature and applied voltage, etc.

### MOSFETs and Diodes

The best performers have been selected for efficiency, size, and cost.

## Application Space Covered by ADIsimPower



This is a graph of the application space covered by ADIsimPower's comprehensive solutions. Output load current is on the x axis and input voltage is on the y axis. You can see the ADP182x family of switching controllers takes up the majority of the area on this screen. This is a tool that is another true Analog Devices' differentiator—no other tool in the industry provides customized and optimized full solutions for synchronous controllers.

Other families of parts included in the ADIsimPower comprehensive solution application space are the ADP210x integrated switching regulators, ADP1864 asynchronous switching controller, and all linear regulators in the ADI portfolio.

Analog Devices has many ICs in power management that cover spaces not shown in this graph. We are in the process of implementing comprehensive solutions for these ICs. The ADIsimPower tool will have quarterly updates, which will add more topologies and more application spaces.

## ADIsimPower Video

## ADIsimPower Step 1: Enter Your Design Criteria

The screenshot shows the ADIsimPower web application interface. At the top is the Analog Devices logo and navigation links. The main heading is 'Design Tools: ADIsimPower™'. Below this is a progress bar with four steps: 1. Enter Your Design Criteria (active), 2. View All Design Solutions, 3. View Solution Details, and 4. Build Your Design. The main content area is titled 'Welcome to ADIsimPower™' and includes a description: 'the most accurate and fastest DC-DC power management design tool!'. Below this is a form titled 'Enter your design criteria or choose the IC you wish to design into your solution.' The form contains five input fields: Vinmin (V) with value 4.5, Vinmax (V) with value 5.5, Vout (V) with value 1.2, Iout (A) with value 0.3, and Tmax (°C) with value 55. Each field has a range constraint below it. There are three buttons: 'Find Solutions', 'Use Dual Channel Device', and 'Clear Fields'. To the right of the form is a graphic showing a circuit schematic with the ADIsimPower logo overlaid. The footer contains links for Privacy/Security, myAnalog, Contact ADI, Site Map, Registration, Technical Support, and Terms of Use, along with a copyright notice for 1995-2008 Analog Devices, Inc.

ADIsimPower will guide you through a four step process, which will result in you receiving a complete solution including schematic, bill of materials, efficiency curves, and other key performance specifications for your application.

### Step 1: Enter Your Design Criteria—

Enter your dc-to-dc power supply design requirements or if you know which IC you'd like to use, you may select it from a drop down list. This will take you directly to the third step, View Solution Details.

You'll enter the range of the input voltage the converter will see in Vinmin and Vinmax.

Enter the output voltage and output current of the converter in the Vout and Iout boxes respectively.

Finally enter the ambient temperature over which the converter must operate.

You can also click dual channel device if you'd like to use an IC that can generate two rails.

# ADIsimPower Step 2: View All Design Solutions

All Fields are required

Vinmin (V)	Vinmax (V)	Vout (V)	Iout (A)	Tmax (°C)
4.5	5.5	1.2	1	55
2.50 ≤ v ≤ 60	2.50 ≤ v ≤ 60	-7 ≤ v ≤ 100	0.001 ≤ v ≤ 50	-40 ≤ v ≤ 125

[Find Solutions](#) [Use Dual Channel Device](#) [Clear Fields](#)

---

**Recommended Solutions**

Criteria	IC	Topology
<a href="#">View Solution</a>	ADP2105	Buck
<a href="#">View Solution</a>	ADP2105	Buck
<a href="#">View Solution</a>	ADP2105	Buck
<a href="#">View Solution</a>	ADP2106	Buck

**ADIsimPower™ has found the best suited ICs for your application!**

- Please pick your primary design goal - Lowest Cost, Smallest Size, Least Parts Count, and Most Efficient and click on the corresponding "View Solution" button.
- If a "View Solution" button is not selectable, a comprehensive design tool does not yet exist. The datasheet will probably have some information to help you out, so click on the part number to learn more.
- Below are other ICs that will work even though they may not be optimized for any of the four main design criteria. You can also filter out ICs that do not have features that are necessary for your application in the check boxes below. If you don't see the feature you need, click "View All Features," and the list will expand.

---

**All Solutions**

Criteria	IC	IC Description	Solution Cost *1 (USD)	Solution Size (mm²)	Efficiency *2 (at load)	Component Count	Topology	Enable Shutdown	Power Good	Tracking	Light Load Efficiency	Synchronous
<a href="#">View Solution</a>	ADP2106	Regulator	1.99	46	0.86	10	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<a href="#">View Solution</a>	ADP2107	Regulator	2.08	46	0.86	10	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<a href="#">View Solution</a>	ADP1821	Controller + Driver	2.78	188	0.82	29	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<a href="#">View Solution</a>	ADP1822	Controller + Driver	2.88	221	0.82	34	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<a href="#">View Solution</a>	ADP1828	Controller + Driver	2.86	213	0.82	22	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<a href="#">View Solution</a>	ADP2105	Regulator	1.87	46	0.82	10	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<a href="#">View Solution</a>	ADP1864	Controller + Driver	2.15	119	0.73	11	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
<a href="#">View Solution</a>	ADP3050	Regulator	2.67	62	0.68	11	Buck	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

[Features](#)  
[Show all features \(17\)](#)

## Step 2: View All Design Solutions—

In this step of the process you'll be able to pick from a list of possible solutions. Performance estimates are given for cost, size, efficiency, and component count for each solution. You can sort by each of these criteria as well as IC Description and Topology. The superlative of each of these design goals is at the top for quick access. A list of the IC features is available in the table at the bottom. You can view only ICs that have the features you want by clicking on the corresponding check box in the features list. If you don't see the feature you require, click on "Show all features" to see all 17 possibilities.

If you click on an IC, you'll get a pop up with various options including View Solution, View Product Page, View Data Sheet, Download Design Tool, Download Eval Board App Note. Once you have found the desired solution click on "View Solution" to go to the next step. If the View Solution button is grayed out, a comprehensive solution does not yet exist.

## ADIsimPower Step 3: View Solution Details

Skip down to: [Bill Of Materials](#) | [Efficiency Graph](#) | [Performance Data](#)

**User Input Data & Solution Schematic** [Build This Solution!](#) [Back to Top](#)

Designed for: ☒ Lowest cost ☐ Part count ☐ Efficiency ☐ Size

User Target Specs Default Design Specs

Spec	Target Value	Actual Value	Units
Vout	1.200	1.209	Volt
Iout	0.300		Amp
Pout	0.360	0.363	Watt
TA	55		°C
Vinmin	4.5		Volt
Vinmax	5.5		Volt

**Bill of Materials** [Download Bill of Materials](#) [Build This Solution!](#) [Back to Top](#)

Designed for: ☒ Lowest cost ☐ Part count ☐ Efficiency ☐ Size

Note: Components with an "Item #" in orange can be changed. To select a different component, click on the item # to edit. Updating components must be done in the order they appear in the BOM.

Item #	Des	Mfg	Part Number	Component Specs	Pkg	Part Qty	Area(mm²)	Hgt(mm)	Cost(\$)*
1	IC1	ADI	ADP1864AUJZ-R7	PFET Controller	TSOT-6	1	9	1	1.060
2	L1	Coilcraft	ME3220-223	22µH, 787mΩ, 0.74pk	Unshielded	1	8	2	0.230
3	Rd1	Susumu	RL1220S-0R24-G	240mΩ	805	1	3.2	0.4	0.036
4	D1	Vishay	BAT54-V	0.2A, 30Vmax, 0.89Vf	SOT23	1	7.6	1.1	0.036
5	Q1	Siliconix	Si2301BDS	100mΩ, 1.25Vth	SOT23-3	1	8.7	1.1	0.170
6	Cin1	Taiyo Yuden	LMK212 BJ106KG-T	10µF, 10V, 7mQ	805	1	2.5	1.3	0.031
7	Cout1	Taiyo Yuden	JMK212 BJ106MG-T	10µF, 6.3V, 7mQ	805	1	2.5	1.3	0.025
8	R1	Vishay	1% tolerance	100kΩ	603	1	1.3	0.4	0.005
9	R2	Vishay	1% tolerance	51.1kΩ	603	1	1.3	0.4	0.005
10	Rc	Vishay	1% tolerance	43.2kΩ	603	1	1.3	0.4	0.005
11	Cc1	Vishay	< 10% tolerance	1nF, X7R	603	1	1.3	1	0.010
12	Cc0	Vishay	< 10% tolerance	15pF, X7R	603	1	1.3	1	0.010
<b>Totals:</b>						<b>12</b>	<b>49</b>	<b>2.0</b>	<b>\$1.62</b>

\* Disclaimer:  
1. BOM prices shown are 1000 piece estimates in US Dollars that should be used for comparison purposes only.  
2. It is the user's responsibility to verify actual design performance through prototyping and test.

### Step 3: View Solution Details—

In the third step or the “View Solution Details” step, you’ll be able to view a schematic, bill of materials, efficiency graph, phase/gain plot, and performance data all customized for your specific input parameters.

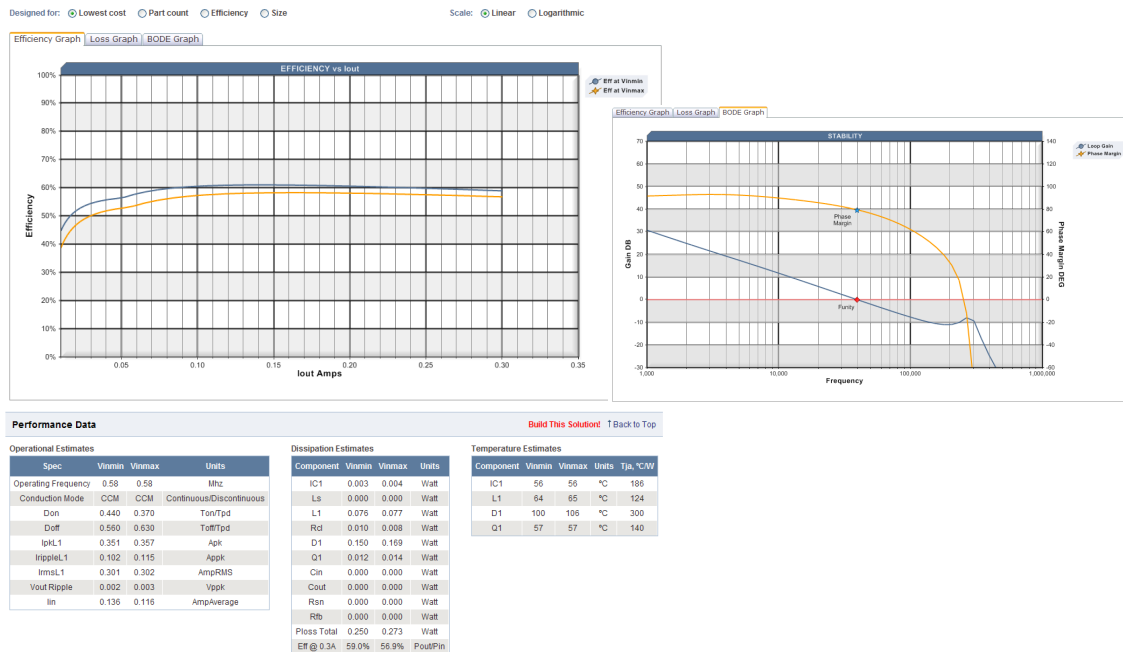
You’ll be able to modify advance settings, which will include many things including but not limited to: output voltage ripple spec, load transient specs, maximum component height, input filter, and switching frequency options.

At the top of each section you’ll be able to change the design goal for your converter. Radial buttons will allow you to optimize for cost, parts count, efficiency, and size. You can watch your bill of materials and efficiency curve change as you select different design goals.

The bill of materials is fully customizable and can be exported to Excel. If the line item is red, you can click on it to see a list of other components that are prequalified to work in your design. As you view the list of parts, you’ll be given many parameters that will help you make your decision including but not limited to: cost, loss, area, height, part number, manufacturer, etc.



## ADIsimPower Step 3: View Solution Details (Continued)

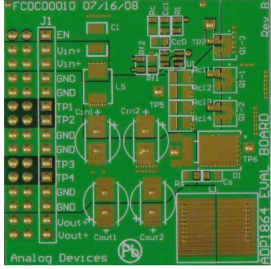


Scrolling down, you'll find an efficiency curve, which predicts the efficiency at the maximum and minimum output voltage. You can switch between log and linear scales depending on the area of interest on the curve. Another tab is the loss graph over load, which is the data from which the efficiency numbers are derived. The third tab in the graph list is the phase/gain analysis that shows the small signal stability of the converter as it is in your customized design.

Below the graphs is the performance data, which will offer predictions about how the converter will operate, power dissipation estimates for each component, and temperature estimates of each of the components.

Once you have finalized your design click on "Build This Solution."

## ADIsimPower Step 4: Build Your Design



**ADP1864-EVALZ**

You've arrived at the final stage of ADIsimPower. Below is all the documentation you need to build your customized design.

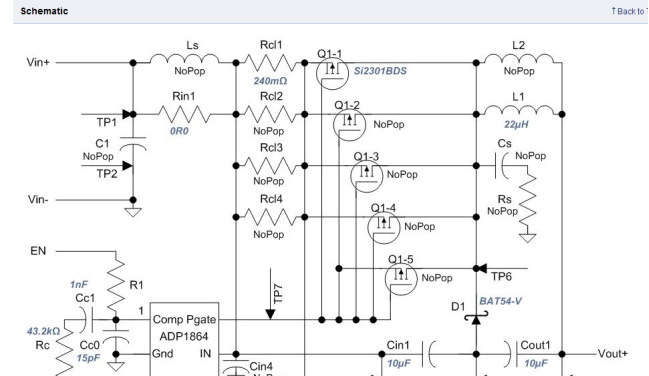
Just click on 'Buy It' to add the ADP1864AUIZ-R7 and the ADP1864-EVALZ to your shopping cart.

The evaluation board often has multiple configuration options that may not be applicable to your particular design, so the Bill of Materials may have more line items than the BOM of the previous page.

If you choose to build your own hardware instead of using the ADP1864-EVALZ below are pictures of each of the PCB layers to guide your layout.

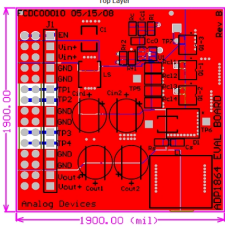
**Purchase Information: ADP1864**

Model	Sample	Purchase
ADP1864AUIZ-R7	Add to Cart	Add to Cart
ADP1864-BL-EVALZ	Add to Cart	Add to Cart



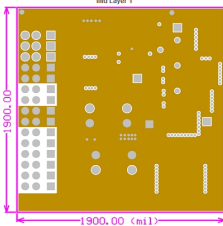
**Schematic**

The schematic shows the power management circuit for the ADP1864-EVALZ. It includes input filters (Ls, Rin1, C1, TP1, TP2), a feedback network (R1, R2, Cc1, R3, Cc2), and output filters (L1, L2, Cs, R4, C4, TP6). The ADP1864 controller is shown with its internal components (Q1-1 to Q1-5, D1, TP7, Cin1, Cout1) and external components (Cin4, Cout1, R4, C4, TP6).



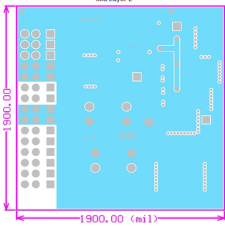
**Top Layer**

1900.00 (mm)



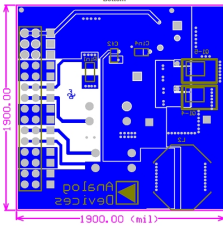
**Mid Layer 1**

1900.00 (mm)



**Mid Layer 2**

1900.00 (mm)



**Bottom**

1900.00 (mm)

### Step 4: Build Your Design—

This is the final step in ADIsimPower.

Here you will be given links to purchase evaluation boards that correspond exactly with the BOM and schematic you received that were customized for your design. You'll see a picture of the evaluation board, a schematic that is complete with component values placed on it (ideal for use in assembling the board), a bill of materials, and layout guidelines.

The schematic and evaluation board accommodate many different configurations, so the BOM and schematic may have quite a few components that you will not be required to populate for your application.

The layout recommendations usually come in the form of the artwork required for each of the PCB layers of the evaluation board.

# Technical Reference Material

## Analog Devices' Textbook References

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. See Chapter 9.
2. Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410. See Chapter 7.
3. Walt Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN: 0-916550-26-5. Also available as *Op Amp Applications Handbook*, Elsevier-Newnes, 2004, ISBN: 0-7506-7844-5. See Chapter 7.

## Other Textbook References

1. Irving M. Gottlieb, *Power Supplies, Switching Regulators, Inverters, and Converters, Second Edition*, McGraw Hill (TAB Books), 1994.
2. Marty Brown, *Practical Switching Power Supply Design*, Academic Press, 1990.
3. Marty Brown, *Power Supply Cookbook*, Butterworth-Heinemann, 1994.
4. John D. Lenk, *Simplified Design of Switching Power Supplies*, Butterworth-Heinemann, 1995.
5. Keith Billings, *Switchmode Power Supply Handbook*, McGraw-Hill, 1989.
6. George Chryssis, *High-Frequency Switching Power Supplies: Theory and Design, Second Edition*, McGraw-Hill, 1989.
7. Abraham I. Pressman, *Switching Power Supply Design*, McGraw-Hill, 1991.

Notes:

## Practical Power Solutions

1. Point-of-Load Power
2. System Power Management and Portable Power
3. Power for Mixed Analog/Digital Systems
4. Hardware Design Techniques

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### SECTION 2

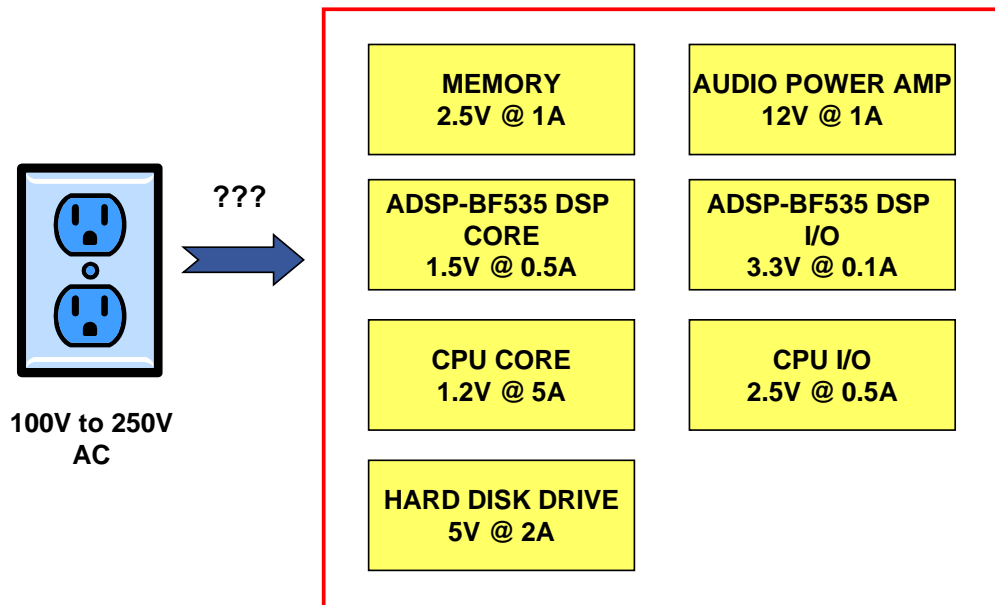
#### SYSTEM POWER MANAGEMENT AND PORTABLE POWER

Designing a Typical System Power Chain.....	2.1
Microprocessor Supervisory Functions.....	2.13
Power Supply Monitoring and Sequencing.....	2.20
Hot Swap Controllers.....	2.32
Temperature Monitoring.....	2.42
Digital Isolation and Isolated Power.....	2.48
Digital Power Applications.....	2.58
Powering Portable Systems.....	2.63
Technical References.....	2.76

## Designing a Typical System Power Chain



## A Typical System Using AC Power



**PEAK VALUES ASSUMED FOR CURRENTS AT NOMINAL VOLTAGES**

In this portion of the seminar, we will examine a typical system and lay out an appropriate power chain.

This system consists of a CPU, DSP (Blackfin ADSP-BF535), an audio power amplifier, and a hard disk drive. Notice that the core and I/O voltages for the CPU and DSP are different—a typical situation often encountered in modern designs.

The various voltages and current requirements are shown in the diagram. The power must come from a standard ac wall outlet (rated at 15 A or 20 A).

It is assumed that the currents above represent maximum currents at the nominal voltages.

## End Power Requirements for System

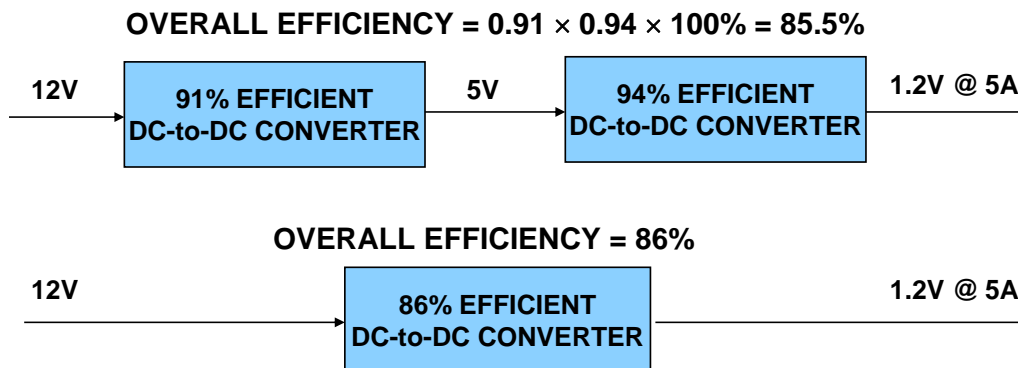
Function	Voltage (V)	Current (A)	Power (W)
Audio Power Amp	12.00	1.00	12.00
CPU Core	1.20	5.00	6.00
CPU I/O	2.50	0.50	1.25
Memory	2.50	1.00	2.50
Hard Disk Drive	5.00	2.00	10.00
ADSP-BF535 DSP Core	1.50	0.50	0.75
ADSP-BF535 DSP I/O	3.30	0.10	0.33
Total Power			32.83

PEAK VALUES ASSUMED FOR CURRENTS AT NOMINAL VOLTAGES

This figure breaks out the various voltages and currents required to power the system. The total power consumed is 32.83 W.

## General Guidelines for Power Trains

- ◆ **Start with higher voltages and regulate down (buck), not up (boost)**
- ◆ **Do not make more voltages than you actually need**
  - **Exception: For a low noise power rail, you may need to pre-regulate the input of an LDO with a buck (or maybe a boost) converter to keep power dissipation in the LDO low**
- ◆ **Do not run the power through more conversions than you need:**



Before starting the design, it is useful to examine several useful guidelines relating to fixed (non-portable) power system design.

As previously discussed, it is wise to distribute higher voltages and then regulate down from them at the points-of-load using buck regulators or LDOs. It is generally unwise to use boost converters in fixed power applications. These are much more suitable for battery-operated portable systems. However, if the current is low enough, a boost converter can be useful in certain applications.

You should also try and design the system with as few voltages as possible; i.e. do not generate intermediate bus voltages that are not used in the system. There is one important exception to this rule where it is desirable to use an LDO to generate a low noise supply voltage, perhaps to power a mixed-signal device such as an ADC, PLL, or other noise-sensitive analog circuit. In this case it may be wise to use a buck converter (in some cases a boost converter) as a pre-regulator for the LDO. The output of the buck or boost converter is made slightly higher than the LDO output voltage plus the LDO dropout voltage. This minimizes power dissipation in the LDO.

Finally, try and minimize the number of power conversions in any given power path. Remember that the overall efficiency of two converters in series is equal to the product of the individual efficiencies. A 91% efficient converter in series with a 94% efficient converter yields a total efficiency of 85.5%.

The example above shows that the 12 V to 1.2 V buck converter is only 86% efficient, primarily because of the high  $V_{IN}/V_{OUT}$  ratio. Even though the individual 12 V to 5 V and 5 V to 1.2 V converters are more efficient (91% and 94%, respectively), their combined efficiency of 85.5% is no better than using the single converter.

## Choice of AC Power Adapter



5V, 9V, 12V, 18V, 24V ????

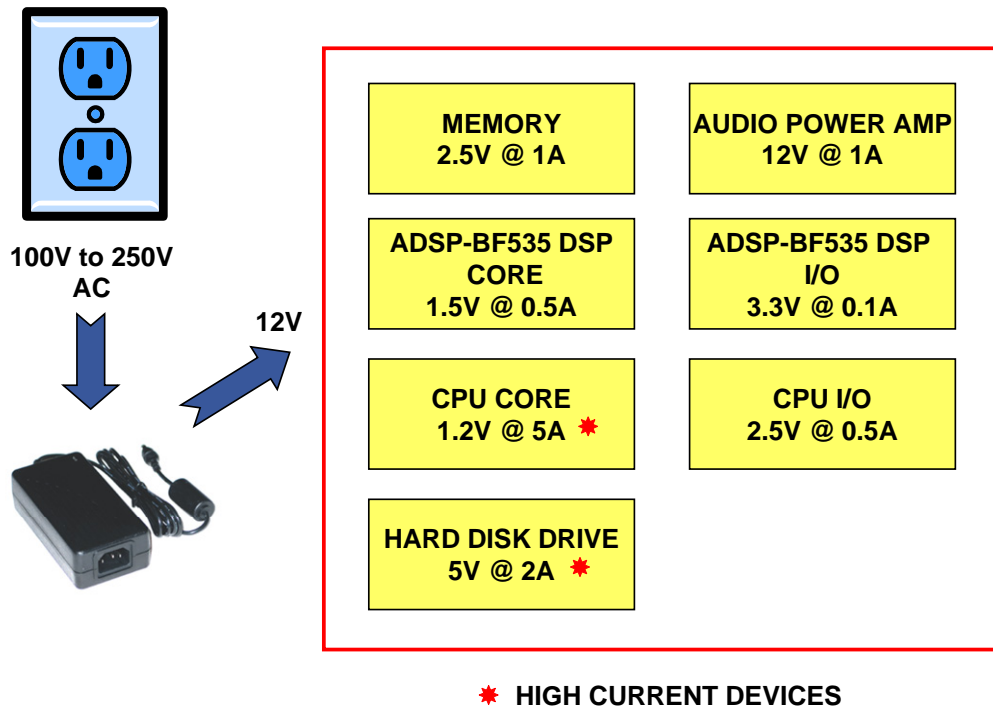
- ◆ This is the largest voltage that we need in the system
- ◆ We don't have to use a separate regulator for the 12V audio amp
- ◆ We can regulate down from here to get the other voltages

The first step in the power design is to select the ac adapter output voltage. These adapters are available with a number of different dc voltage outputs.

We will select a 12 V adapter because 12 V can be used directly by the power amplifier. This way the power amplifier does not need its own regulator. Here we are assuming that after proper filtering, the 12 V supply is "quiet" enough to power the audio amplifier.

The 12 V output can be regulated down to get the other voltages required in the system.

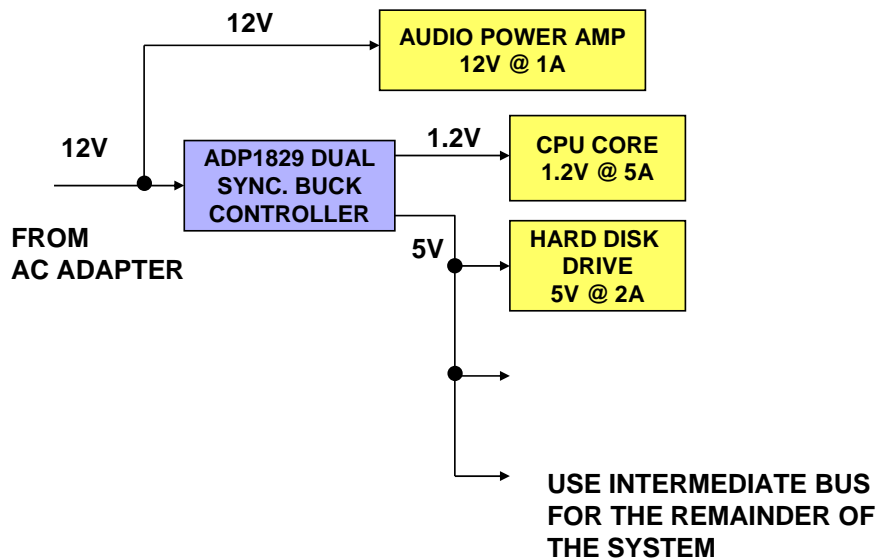
## After Choosing a 12V Power Bus, What is the Next Step?



Now that 12 V has been chosen as the primary dc bus, what is the next step in the design?

A good place to start is to examine the requirements for the voltages which require the largest current: the 1.2 V CPU core voltage (5 A) and the 5 V hard disk drive (2 A).

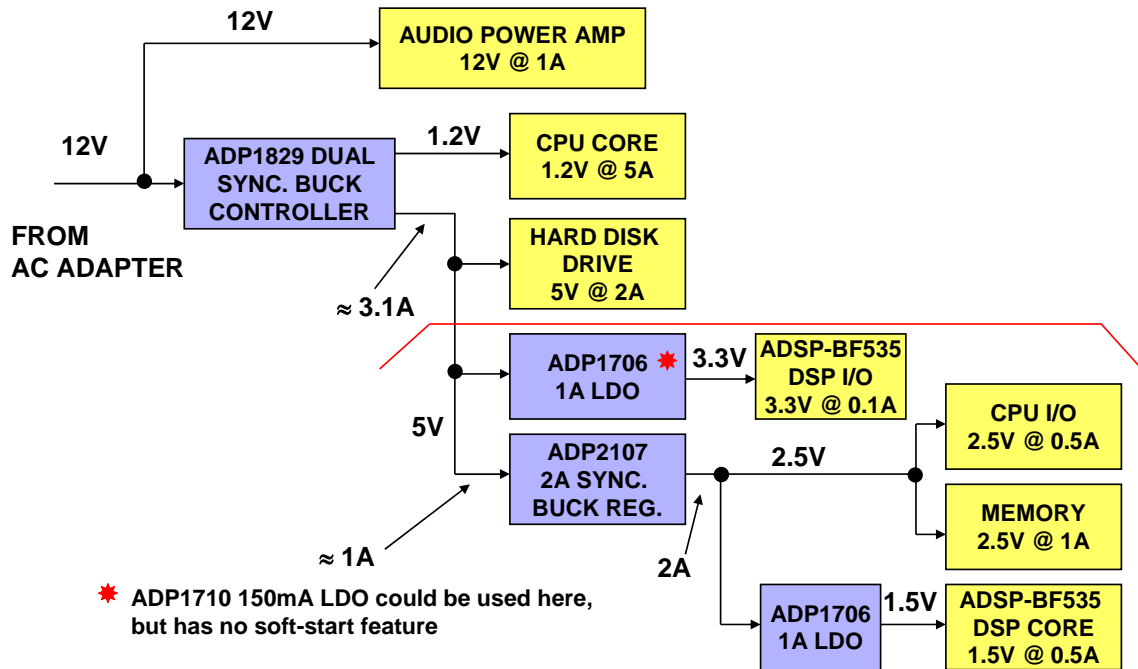
## Powering the High Current Devices from a Dual Synchronous Buck Controller



Since there are two relatively high current rails, a dual synchronous buck controller such as the ADP1829 can be used to generate both the 5 V and 1.2 V rails from the 12 V input. The 5 V rail can then be used as an intermediate bus to generate the lower voltages required in the system.

Although it would be possible to generate the 1.2 V CPU core voltage from the intermediate 5 V bus, this puts two high current regulators in series, and the overall efficiency will be no better than generating the 1.2 V directly from the 12 V rail.

## Finishing the Design using the 5V Intermediate Bus and More POL Regulators



Continuing with the design, we will use an LDO to generate the 3.3 V required for the DSP I/O because the current requirement is only 0.1 A. The ADP1710 150 mA low cost LDO comes in a 5-lead TSOT package and has a worst case  $\theta_{JA} = 170^{\circ}\text{C}/\text{W}$  (assuming no surrounding copper area). In the circuit the part dissipates 0.17 W, giving a  $29^{\circ}\text{C}$  rise from ambient-to-junction. Although this is more than adequate for operation at  $85^{\circ}\text{C}$  ambient, the ADP1710 does not have a soft-start feature which might be needed for sequencing.

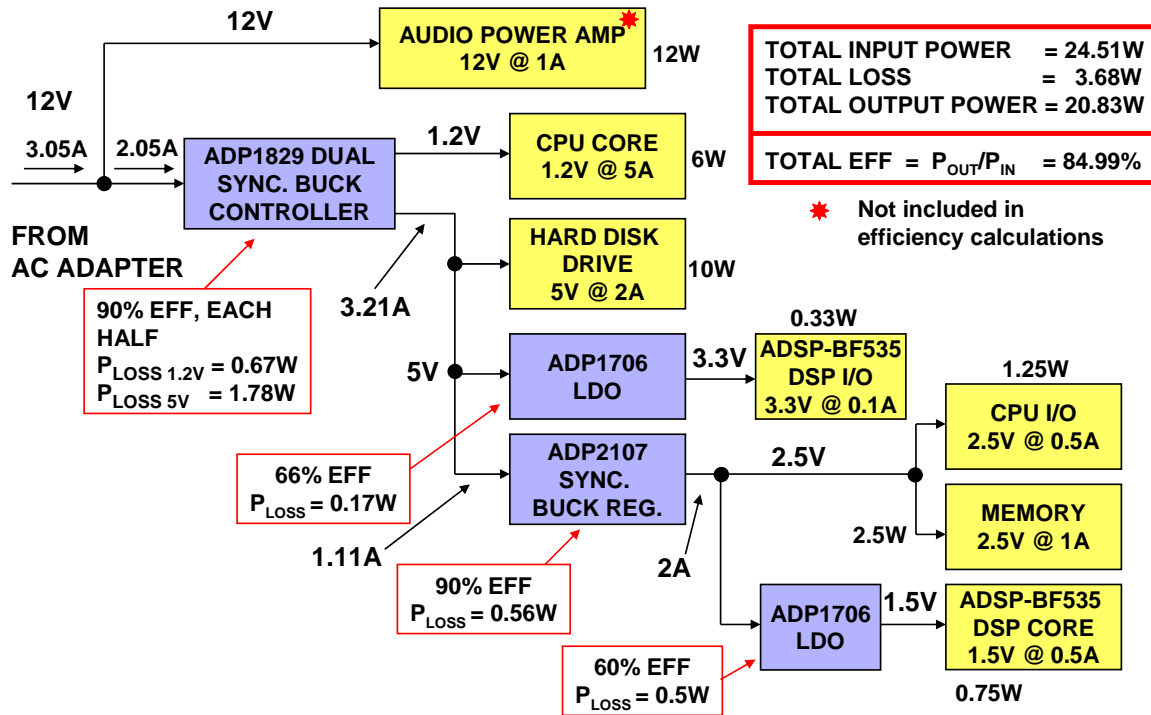
The ADP1706 handles 1 A and has a worst case  $\theta_{JA}$  of  $58^{\circ}\text{C}/\text{W}$  in the 8-lead, exposed paddle SOIC; and a worst case  $\theta_{JA}$  of  $66^{\circ}\text{C}/\text{W}$  in the 8-lead exposed paddle LFCSP. This part is rated for 1 A and has a soft-start feature.

We will use the ADP2107 2 A synchronous buck regulator to generate the 2.5 V for the CPU I/O and the memory.

The ADP1706 LDO is used to generate the 1.5 V core voltage for the DSP. In the circuit, the ADP1706 dissipates 0.5 W, so this yields an ambient to junction rise of  $33^{\circ}\text{C}$  using  $\theta_{JA} = 66^{\circ}\text{C}/\text{W}$ .

In order to maintain parts commonality and to allow for soft-start capability, we will use the ADP1706 LDO in both applications.

## Overall System Efficiency Calculations



Here we have calculated the individual power losses for both the switching converters and the LDOs. An efficiency of 90% was assumed for the switching converters. The power dissipated in the LDOs was calculated by multiplying the LDO  $V_{IN} - V_{OUT}$  by the output current.

The first step is to calculate the input currents for the switching converters based on their efficiency.

The total efficiency of the system is calculated by taking the ratio of the output power (power dissipated in the actual system blocks in yellow) to the input power (total system power dissipation including regulator losses). The efficiency works out to be a respectable 84.99%.

The 12 watts dissipated by the audio power amplifier is not counted in the efficiency calculations because it is powered directly from the ac adapter output. The total efficiency calculation does not include the efficiency of the ac adapter.



## Efficiency Comparison: ADP2107 Synchronous Regulator vs. ADP1864 Asynchronous Controller

- ◆ **ADP2105/ADP2106/ADP2107: Synchronous Buck Regulator, Internal Switches**
  - Optimized for output currents of 1A (ADP2105), 1.5A (ADP2106), and 2A (ADP2107).
  - $V_{IN} = 2.7V$  to  $5.5V$ ,  $V_{OUT} = 0.8V$  to  $V_{IN}$
  - Synchronous gives good efficiency for higher currents, low voltages
  - 1.2MHz Switching Frequency
  - For output currents less than 0.6A, ADP2102 or ADP2108 regulators offer compact solutions at 3MHz switching frequencies
- ◆ **ADP1864: Asynchronous Buck Controller, External PMOS FET and Schottky diode**
  - $V_{IN} = 3.15V$  to  $14V$ ,  $V_{OUT} = 0.8V$  to  $V_{IN}$
  - Generally used for outputs up to 5A
  - Diode limits efficiency for high currents, low output voltages
  - 580kHz Switching Frequency

For output currents less than a few amps, a synchronous buck regulator is a good choice, such as the ADP2105 (1 A), ADP2106 (1.5 A), and ADP2107 (2 A). The switches are integrated, and the parts therefore require only a few external components for a complete design. The synchronous switch gives good efficiency, especially for higher currents and low output voltages.

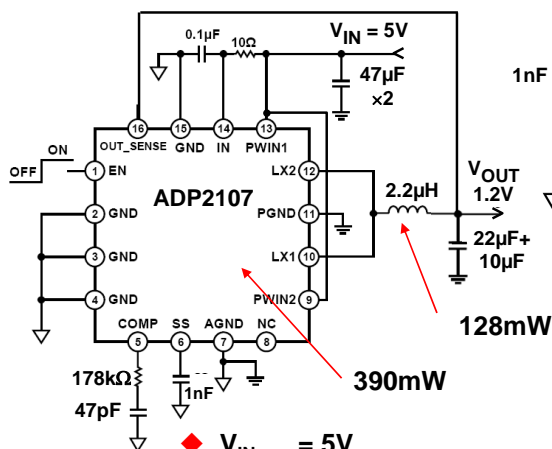
For currents of 600 mA or less, the ADP2102 and ADP2108 offer compact solutions because of their 3 MHz switching frequencies.

On the other hand, an asynchronous buck regulator using external components, such as the ADP1864, can be configured to supply more output current with a higher parts count and larger size. The ADP1864 is useful for output currents up to about 5 A.

In this exercise, we will let ADIsimPower create two designs. The first design uses the ADP2107 synchronous regulator, and the second design uses the ADP1864 asynchronous buck controller. The ADIsimPower designs allow comparisons between the efficiency, cost, and board space for the two approaches.

## Design Solutions Using ADIsimPower

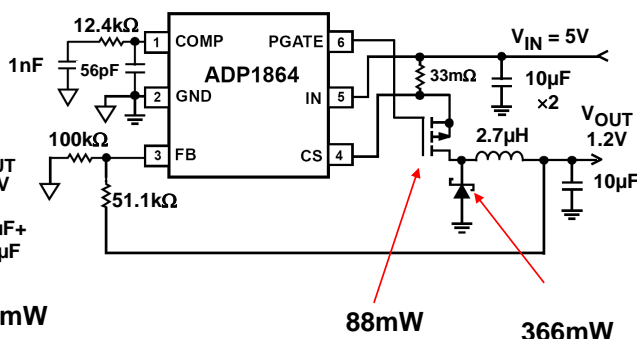
### ADP2107 DESIGN



- ◆  $V_{IN} = 5V$
- ◆  $V_{OUT} = 1.2V @ 2A$
- ◆  $P_{OUT} = 2.4W$
- ◆  $P_{LOSS} = 530mW$
- ◆  $EFF = 82\%$

- ◆  $COST \approx \$2.63$
- ◆  $AREA \approx 74mm^2$

### ADP1864 DESIGN



- ◆  $V_{IN} = 5V$
- ◆  $V_{OUT} = 1.2V @ 2A$
- ◆  $P_{OUT} = 2.4W$
- ◆  $P_{LOSS} = 516mW$
- ◆  $EFF = 82\%$

- ◆  $COST \approx \$3.02$
- ◆  $AREA \approx 333mm^2$

The design parameters entered into the ADIsimPower online design tool are:

1.  $V_{OUT} = 1.2V$
2.  $I_{OUT} = 2A$
3.  $V_{INMIN} = 5V$
4.  $V_{INMAX} = 5V$
5.  $T_{MAX} \text{ Ambient} = 50^{\circ}C$
6. Optimize design for Efficiency (other choices are Lowest cost, Lowest Part count, and Smallest Size). Note that the design tool optimizes efficiency at the maximum specified current.

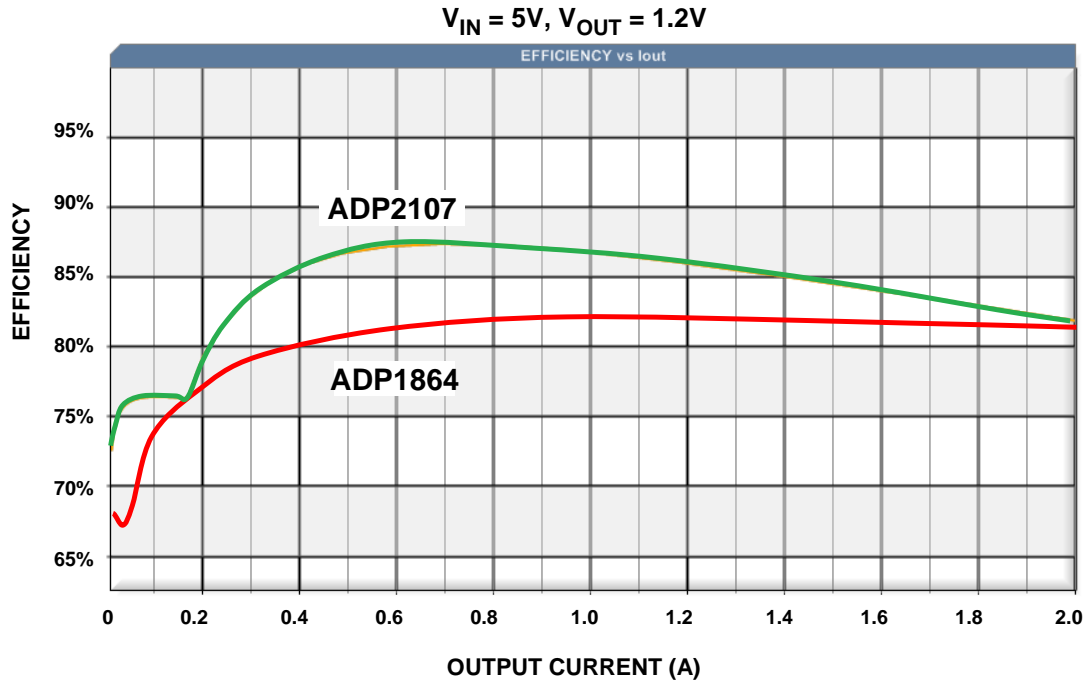
The figures above show the two designs obtained from ADIsimPower, which also gives a complete bill-of-material, thermal analysis, and parts cost.

To calculate efficiency, we must know the power losses. From ADIsimPower, the AD2107 design dissipates the largest amount in the IC itself due to the internal switching losses.

In the ADP1864 design, the two largest power loss contributors are the PFET switch (three Siliconix SI235DS FETs in parallel) and the free-wheeling Schottky diode (IR/Vishay 30BQ015).

Overall efficiency of the two designs at 2 A output current is approximately the same, but the ADP1864 solution costs more and takes up about 5 times the area of the ADP2107 solution. Efficiency of the ADP2107 design is much better than the ADP1864 design at lower currents.

## Efficiency of ADP1864 Asynchronous Buck Controller vs. ADP2107 PFM Synchronous Buck Regulator



This shows the efficiency of the two designs from output currents of 10 mA up to 2 A.

The ADP2107 smoothly transitions from the PWM (pulse width modulation) mode to the variable frequency PFM (pulse frequency mode) mode of operation when the load current decreases below the pulse-skipping threshold current, switching only as necessary to maintain the output voltage within regulation. When the output voltage first dips below regulation, the ADP2107 enters the PFM mode for a few oscillator cycles to increase the output voltage back to regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies all the load current. Because the output voltage dips and recovers occasionally, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

The output current at which the ADP2107 transitions from variable frequency PFM control to fixed frequency PWM control is called the pulse-skipping threshold. The pulse-skipping threshold has been optimized for excellent efficiency over all load currents.

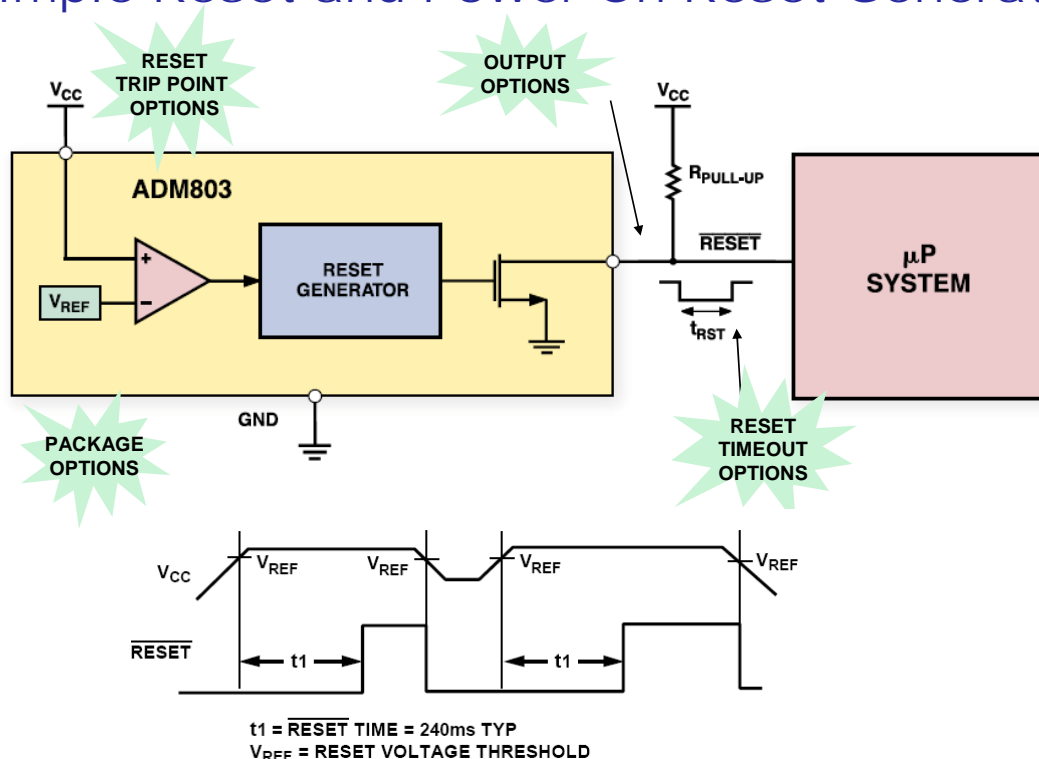
The efficiency of the ADP1864 design is not as good at low currents, and the cost, parts count, and area is greater.

The obvious conclusion is that it is better to use a fully integrated PFM synchronous regulator where possible for currents of a few amps or less.

# Microprocessor Supervisory Functions

[www.analog.com/supervisory](http://www.analog.com/supervisory)

## Simple Reset and Power-On Reset Generator



The initial state of a microprocessor after power-up must be predictable and repeatable. After power-up, a momentary out-of-limit voltage on the power supply can cause processing errors. For these reasons, some type of microprocessor supervisory circuit is generally used as a reset generator or power-on reset generator.

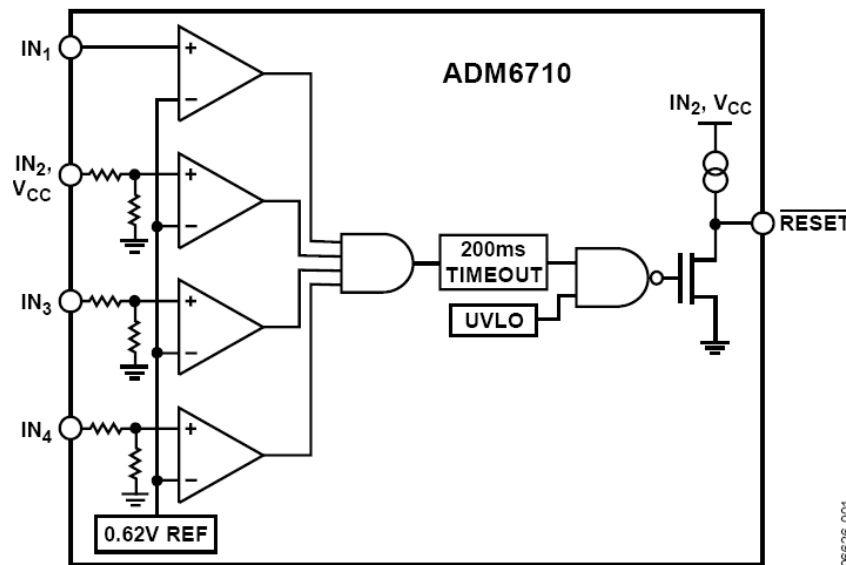
The simplest form of the power-on reset generator is shown in this figure. The ADM803 supervisory circuit monitors the power supply voltage in microprocessor systems. It provides a reset output during power-up, power-down, and brownout conditions. On power-up, an internal timer holds the RESET asserted for 240 ms. This holds the microprocessor in a reset state until conditions have stabilized. The RESET output remains operational with  $V_{CC}$  as low as 1 V. The ADM803 and ADM809 provide an active low reset signal, while the ADM810 provides an active high reset signal output. The ADM809 and ADM810 have push-pull outputs, whereas the ADM803 has an open-drain output which requires an external pull-up resistor.

Seven reset threshold voltage options are available, suitable for monitoring a variety of supply voltages.

The reset comparator features built-in glitch immunity, making it immune to fast transients on  $V_{CC}$ .

The ADM803/ADM809/ADM810 consume only 17  $\mu A$ , making them suitable for low power, portable equipment. The ADM803 is available in a 3-lead SC70; the ADM809/ADM810 are available in 3-lead SOT-23 and SC70 packages.

## ADM6710 Low Voltage Quad Supervisory Circuit



Many modern microprocessors require a separate core and I/O voltage. There may be other critical voltages in the system which need monitoring for out-of-limit conditions.

The ADM6710 is a low voltage, high accuracy supervisory circuit which monitors up to four system supply voltages.

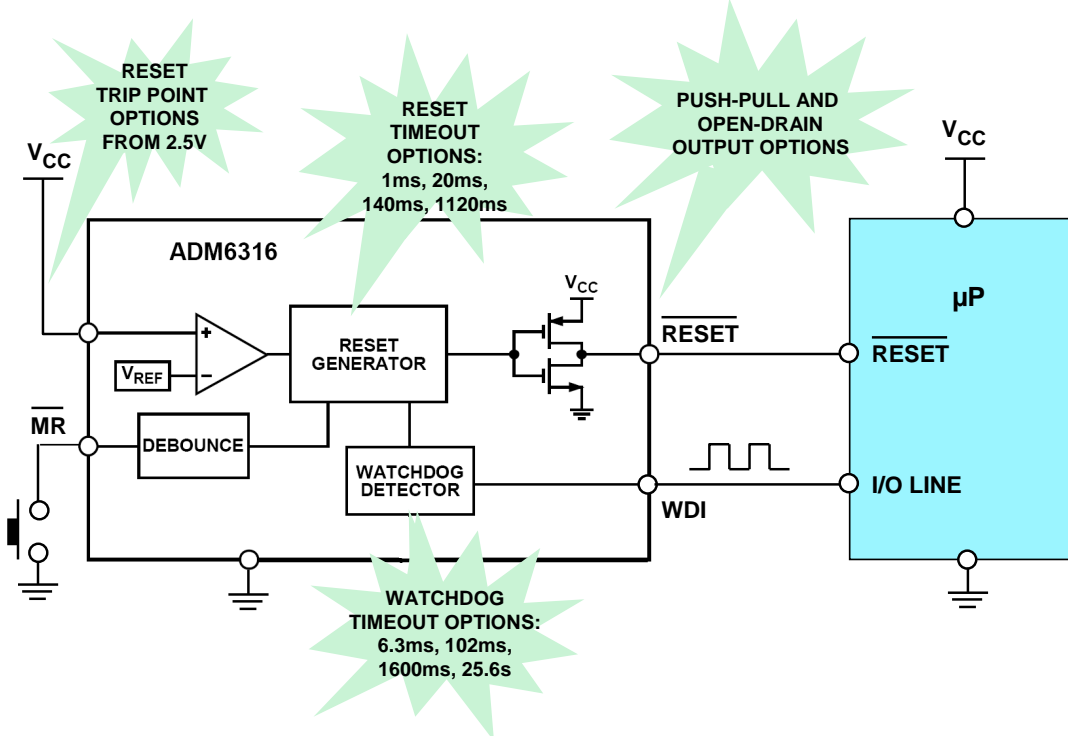
The ADM6710 incorporates a variety of internally pre-trimmed undervoltage threshold options for monitoring 1.8 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V supply voltages. The ADM6710Q offers three adjustable thresholds for monitoring voltages down to 0.62 V.

If a monitored power supply voltage falls below the minimum voltage threshold, a single active low output asserts, triggering a system reset. The output is open drain with a weak internal pull-up to the monitored IN2 supply (or to  $V_{CC}$  in the case of the ADM6710Q) of typically 10  $\mu A$ . Once all voltages rise above the selected threshold level, the reset signal remains low for the reset timeout period (200 ms typical).

The ADM6710 output remains valid as long as IN1 or IN2 exceeds 1 V, whereas for the ADM6710Q, the output remains valid as long as  $V_{CC}$  exceeds 2 V.

Unused monitored inputs should not be allowed to float or to be grounded, instead they should be connected to a supply voltage greater than their specified threshold voltages. The ADM6710 is available in a 6-lead SOT-23 package.

## Adding an External Reset and a Watchdog Timer to the Reset Generator

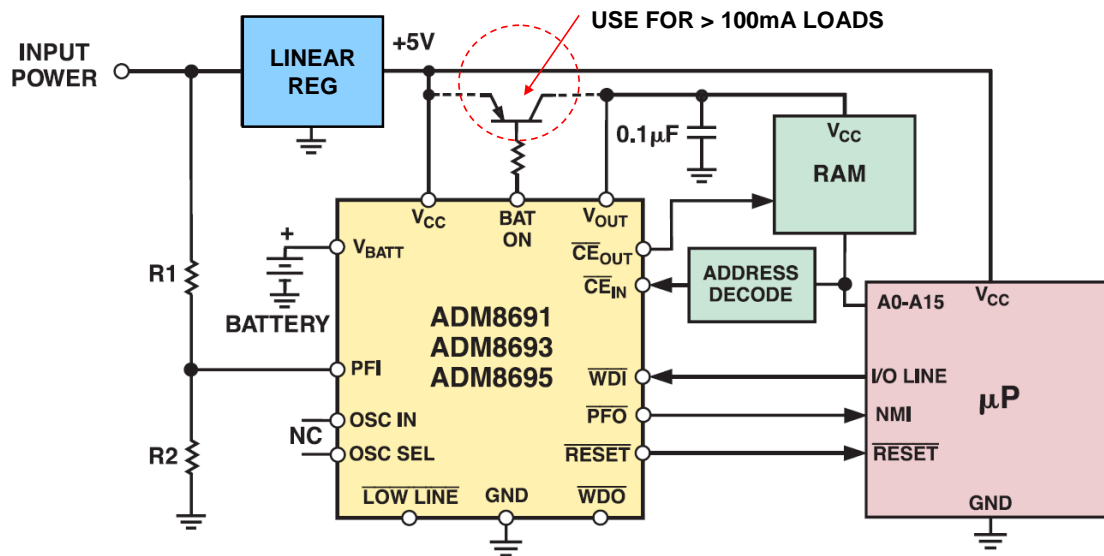


A wide range of reset generator circuits are available designed for use in microprocessor-based systems to monitor power supply voltage levels from 5 V down to 1.58 V. Their reset output signals are asserted whenever the supply voltage falls below a preset threshold level. Reset remains active for a fixed timeout period after the supply voltage has returned to a valid level, so that the supply has time to stabilize before the microprocessor starts up again.

The various models provide a choice of active low or active high and push-pull or open-drain output stages.

Microprocessors need to be reset when code execution errors occur, as well as when supply voltages fall to invalid levels. A watchdog function can detect code execution errors by monitoring frequent logic transitions on a microprocessor's output pin. If a transition is not detected within a certain time period, the watchdog circuit will initiate a reset signal that will take the microprocessor out of its invalid state. Many reset generator/watchdog circuits also feature a power fail detection comparator that asserts an active low signal when the unregulated power supply voltage falls below a predetermined level. This power fail output can be used to generate an interrupt, which allows the microprocessor to implement a shutdown procedure before power is lost.

## Reset Generator and Battery Backup Circuit



A battery backup circuit can be easily controlled with a supervisory circuit by adding an internal PMOS-based switch. In the above circuit, the battery switchover circuit compares  $V_{CC}$  to the  $V_{BATT}$  input, and connects  $V_{OUT}$  to whichever is higher. Switchover occurs when  $V_{CC}$  is 50 mV higher than  $V_{BATT}$  as  $V_{CC}$  falls, and when  $V_{CC}$  is 70 mV greater than  $V_{BATT}$  as  $V_{CC}$  rises. This 20 mV of hysteresis prevents repeated rapid switching if  $V_{CC}$  falls very slowly or remains nearly equal to the battery voltage.

During normal operation, with  $V_{CC}$  higher than  $V_{BATT}$ ,  $V_{CC}$  is internally switched to  $V_{OUT}$  through an internal PMOS switch. This switch has a typical on resistance of  $0.7 \Omega$  and can supply up to 100 mA at the  $V_{OUT}$  terminal.  $V_{OUT}$  is normally used to drive a RAM memory bank. If instantaneous currents of greater than 100 mA are required, a  $0.1 \mu F$  bypass capacitor should be connected to  $V_{OUT}$ . The capacitor provides the peak current transients to the RAM.

If the continuous output current requirement at  $V_{OUT}$  exceeds 100 mA, or if a lower  $V_{CC} - V_{OUT}$  voltage differential is desired, an external PNP pass transistor can be connected in parallel with the internal transistor as shown above with the dotted connection. The **BAT ON** output (ADM8691/ADM8693/ADM8695) can directly drive the base of the external transistor.

These devices also provide the traditional power-on reset and watchdog timer functions in addition to the battery backup function.



## On-Line Supervisory Parametric Search

### Parametric Search - Supervisory

Found 5 Applicable Models. [Jump to Results.](#)

#### Settings for Single Supervisors

Search in: ☒ Available Models ☐ All Models (includes unreleased)

Reset Trip Point (TP) typical (V)	Minimum Reset Timeout (RTO) minimum (ms)	Watchdog	Manual Reset	Reset Output Active-Low	Reset Output Active-High
3	100	Watchdog Input	Yes	Open Drain	Don't Care
Package Type		Watchdog Timeout (WTO) typical (ms)	Power Fail Comparator	Range of Operating Temperature (°C)	
Don't Care 3 MSOP Lead Count Package		150	Yes	Minimum <= -40 Maximum >= 85	

Search for Single Supervisors

Reset Settings

[Contact ADI Experts about Supervisors](#)

See All Results for: [Dual \(2\) Supervisors](#) | [Triple \(3\) Supervisors](#) | [Quad \(4\) Supervisors](#) | [Battery Backup](#)

Because of the wide variety of options available in supervisory products, some type of selection tool is mandatory in order to select the proper part for a specific application.

The online Supervisory Parametric Search performs parametric searches on all Analog Devices supervisory products, both those currently available, and those that can be ordered. Searches can be performed on trip points, reset timeouts, watchdog timeouts, reset types, and other features. This figure shows the opening screen of the search function where the data is entered.

In addition, a general ADI website tool provides cross-referencing between Analog Devices and competitive parts.

## Results from Supervisory Parametric Search

Found 5 Applicable Models

[Export to Excel](#)

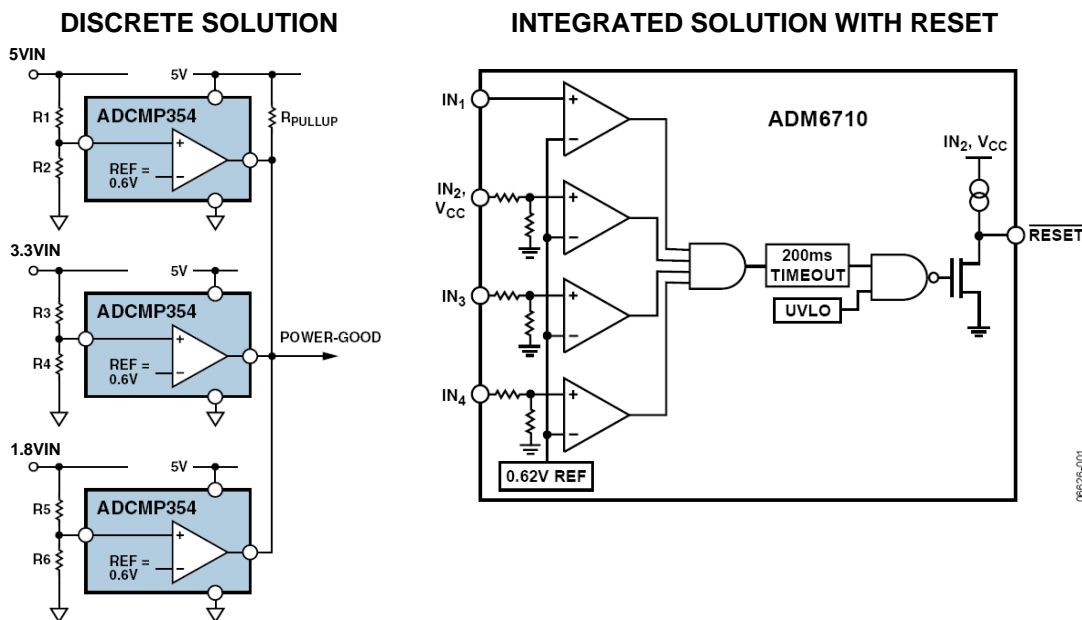
Model	TP1 Typical (V)	TP1 % Accuracy	TP2 Typical (V)	TP2 % Accuracy	RTO min (ms)	Manual Reset	WTO min (ms)	Reset Polarity	Output Structure	Lead Count	Package	Temp min (°C)	Temp max (°C)	ICC max (μA)	Vcc min (V)	Vcc max (V)	Monitored Voltages	PFC	Price \$ (1000 pcs.)	Availability
<a href="#">ADM13305-18ARZ</a>	2.93	2.4	1.68	2.4	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	<a href="#">Available</a>
<a href="#">ADM13305-25ARZ</a>	2.93	2.4	2.25	2.2	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	<a href="#">Available</a>
<a href="#">ADM13305-33ARZ</a>	4.55	2	2.93	2.4	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	<a href="#">Available</a>
<a href="#">ADM13305-4ARZ</a>	2.93	1	0.6	0.8	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	<a href="#">Available</a>
<a href="#">ADM13305-5ARZ</a>	2.25	0.9	0.6	0.8	140	Yes	1600	Active Low & Active High	Push Pull	8	NSOIC	-40	85	40	2.7	5.5	2	-	0.96	<a href="#">Available</a>

After entering the inputs, the parametric search narrows the list of products based on the inputs. In this manner, the proper part can be easily chosen for a specific application.

# Power Supply Monitoring and Sequencing

[www.analog.com/sequencing](http://www.analog.com/sequencing)

## Comparators as Voltage Monitors



This shows a simple method for monitoring multiple voltage rails using the ADCMP354 comparator and reference IC. An individual circuit is used for each rail. Resistive dividers scale the voltage rails down, setting an undervoltage trip point for each supply. All outputs are tied together to generate a common power-good signal as shown in the diagram.

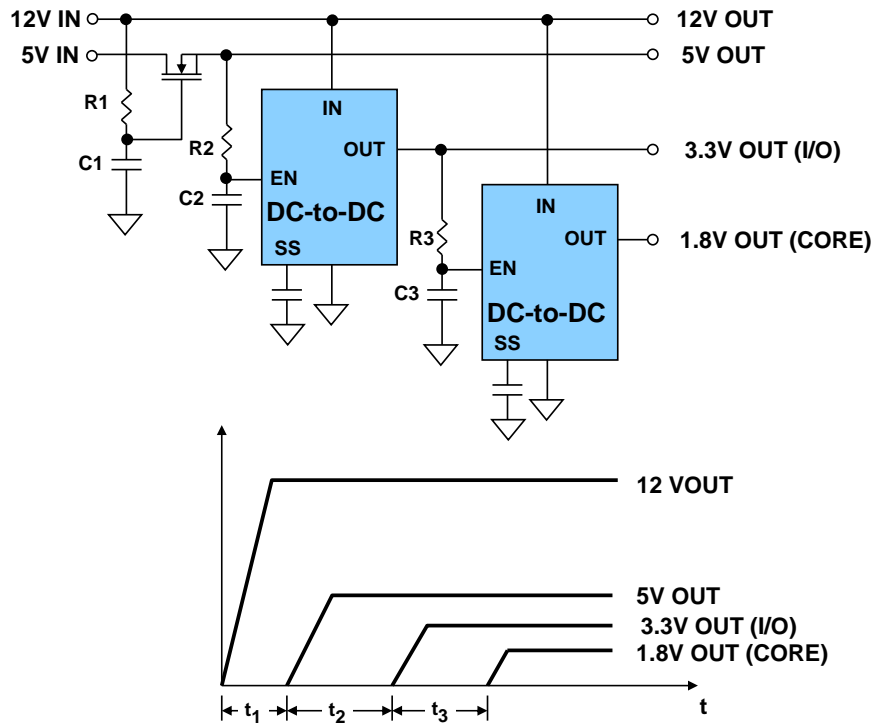
As previously discussed, supervisory circuits integrate the comparators as well as the reset generator in a single IC, such as the ADM6710.

These simple supervisory monitoring and reset functions may be sufficient for many systems. However, in systems with complex digital processors, memory, and multiple supply rails, power rails may require sequencing not only to prevent damage but to ensure proper initialization of various circuits. This problem becomes more complex as the number of supply rails increases.

In some cases it is not possible to predict the exact optimum sequencing order during the early design phases of a project, especially when working with the latest devices (such as FPGAs) which may not have complete characterization data available. In other cases, last minute changes in the design can affect the optimum power supply sequence, illustrating the need for flexible solutions.

The following section addresses several methods for solving these types of monitoring and sequencing problems.

## Sequencing Supplies: I/O Before Core



In this circuit, we use discrete components in conjunction with the Enable (EN) inputs of the dc-to-dc converters to perform a simple sequencing function. In this circuit, the desired sequence is 12 V, 5 V, 3.3 V (processor I/O), and 1.8 V (processor core).

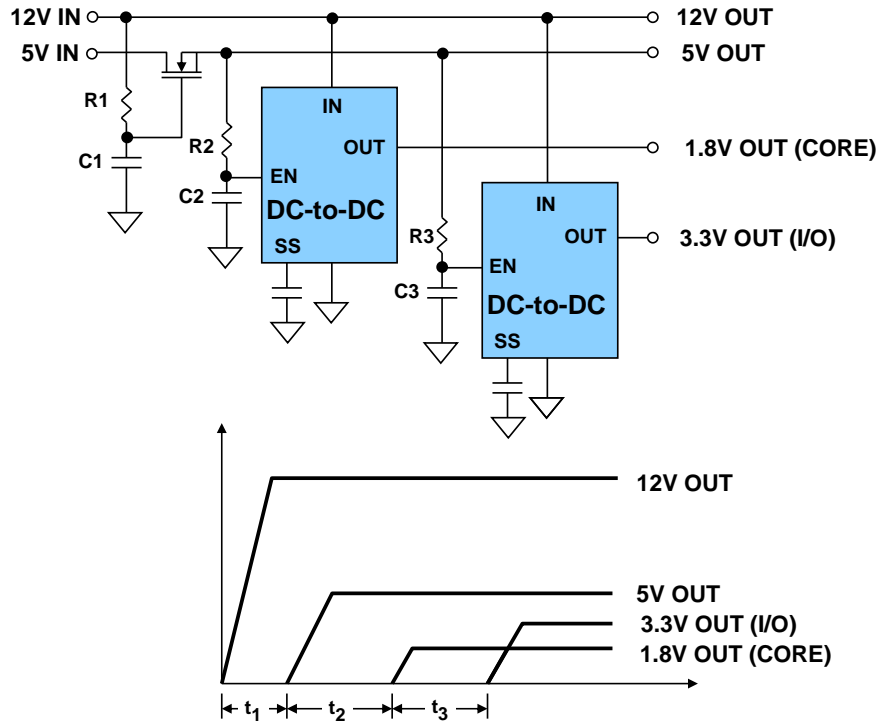
Assume that the 12 V and 5 V input buses come up simultaneously. The R1-C1 network delays the gate drive signal to the NMOS FET which is derived from the 12 V input bus.

The R2-C2 network delays the application of the Enable signal to the 3.3 V I/O dc-to-dc converter.

The output of the 3.3 V dc-to-dc converter is delayed by the R3-C3 network and ultimately enables the 1.8 V core dc-to-dc converter. Note that the 1.8 V supply cannot be enabled before the 3.3 V supply.

The ramp-up slope of the 3.3 V and 1.8 V dc-to-dc converter outputs can be controlled using the Soft Start (SS) functions, if desired to reduce inrush currents.

## Sequencing Supplies: Core Before I/O



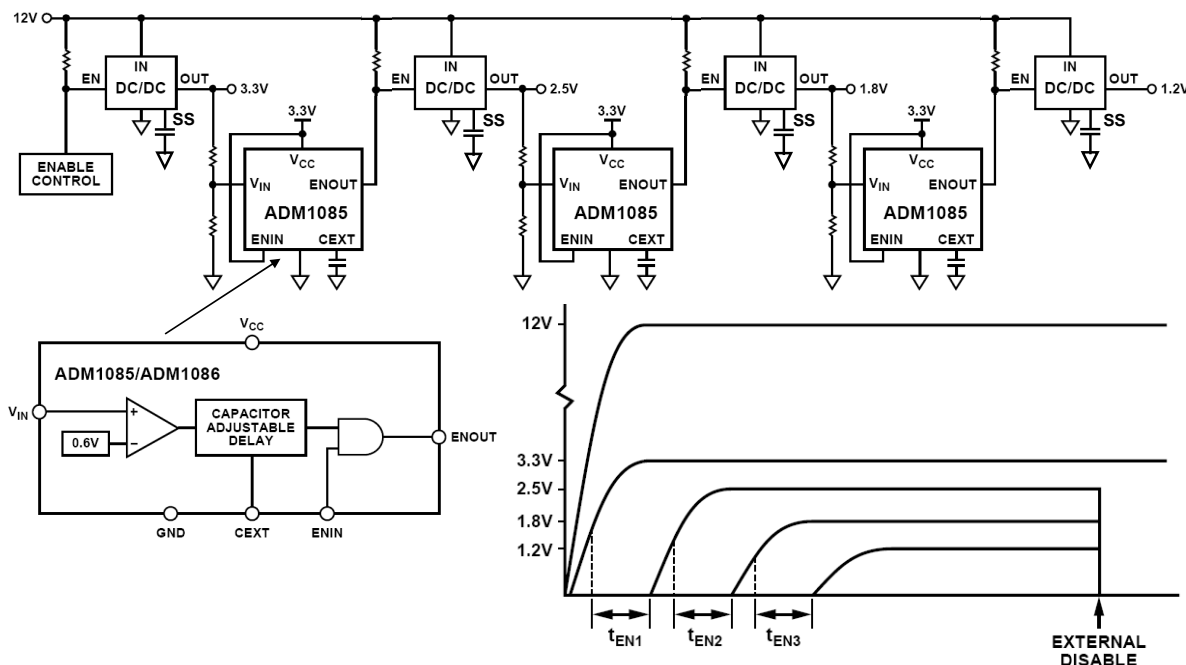
This circuit is similar to the previous one, except the 1.8 V core voltage is brought up before the 3.3 V I/O voltage.

The 3.3 V I/O voltage is enabled using the R3-C3 delay network which is powered from the 5 V bus output.

The proper sequence of the core voltage with respect to the I/O voltage is determined by the particular processor used. In most cases, the core voltage is brought up before the I/O in order to prevent invalid data on the I/O lines, but the processor data sheet should be carefully checked in each case.

Rather than use external discrete components to control sequencing, more integrated solutions are discussed in the next few pages. These ICs offer much more flexibility and accuracy in solving sequencing problems in multirail systems.

## Basic Sequencing Using ADM1085 Simple Sequencer® and Regulator Enables



Here, three ADM1085 Simple Sequencers are used to sequence four individual supplies on power-up. The ADM1085 block diagram is also shown. The device consists of a comparator, capacitor-controlled adjustable delay, and an output stage, very similar to a microprocessor power-on reset circuit. The threshold voltage is set by the resistor divider which scales the particular supply voltage to the internal comparator reference voltage of 0.6 V. The positive-going threshold is 0.56 V to 0.64 V, and the negative-going threshold is 0.545 V to 0.645 V (over the operating temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ). The accuracy of the 0.6 V threshold is approximately 7% over the full operating temperature range. The ADM1085 family of parts are in a 6-lead SC-70 package.

The delay is determined by the value of the capacitor on the CEXT pin. Separate capacitors on the CEXT pins determine the time delays between enabling of the 3.3 V, 2.5 V, 1.8 V, and 1.2 V supplies. Because the dc-to-dc converters and ADM1085s are connected in a cascade, and the output of any converter is dependent on that of the previous one, an external controller can disable all four supplies simultaneously by disabling the first dc-to-dc converter in the chain.

For power-down sequencing, an external controller dictates when the supplies are switched off by accessing the ENIN inputs individually.

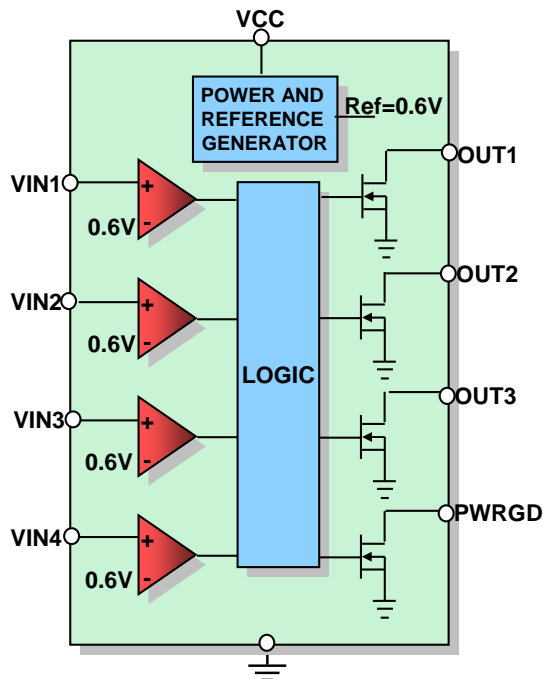
The ADM1085/ADM1086/ADM1087/ADM1088 are compatible with voltage regulators and dc-to-dc converters that have active high or active low enable or shutdown inputs, with a choice of open-drain or push-pull output stages.

The sequence of the supplies is easily changed by simply changing the position of the dc-to-dc converter in the chain and adjusting the divider resistors appropriately.

The dc-to-dc converter soft-start (SS) function can be used to control the individual power supply ramp rates if desired to reduce inrush currents.

## ADM1185 Quad Voltage Monitor & Sequencer

- ◆ **4 Monitoring Comparators :**
  - 0.6V Reference, 0.8% Accurate
  - Trip points set with external resistor dividers
- ◆  **$V_{CC}$  : 2.7V to 5.5V**
- ◆ **4 Open-Drain Outputs:**
  - Three Enable Outputs for Regulators
  - Power Good Output (PWRGD)
- ◆ **Logical Core:**
  - Provides power supply sequencing and fault detection
- ◆ **Package:**
  - 10-lead MSOP
  - Industry's smallest Quad Sequencer



Rather than using an individual Simple Sequencer for each supply voltage as previously described, the ADM1185 allows monitoring and sequencing of up to four supplies. The part contains four individual comparators that are 0.8% accurate as well as a pre-programmed state machine for sequencing.

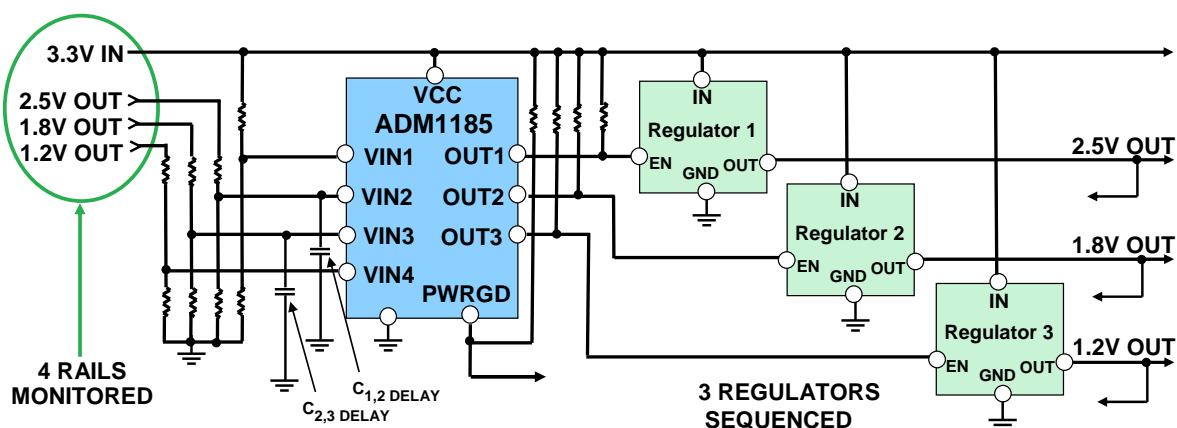
The hardwired logical state machine core interprets the status of the comparator outputs. Internal time delays can be used for sequencing the startup of subsequent power supplies enabled by the outputs. Supplies falling out of range are also detected and, as a result, appropriate outputs are disabled.

The ADM1185 has four open drain outputs. In a typical configuration, OUT1 to OUT3 are used to enable power supplies, while PWRGD is a common power-good output indicating the status of all monitored supplies, i.e., all four comparators are high.

It is important to note that as processor core voltages decrease, the accuracy required to reliably monitor them increases. ADI provides voltage monitoring and sequencing products with accuracies as good as 0.8%.



## ADM1185 Typical Monitoring & Sequencing Application



State	State Name	OUT1	OUT2	OUT3	OUT4	Next Event	Next State
1	Reset	0	0	0	0	VIN1 high for 190 ms	OUT1 On
2	OUT1 On	1	0	0	0	VIN1 and VIN2 high for 30 $\mu$ s	OUT1, OUT2 On
3	OUT1, OUT2 On	1	1	0	0	VIN1 and VIN3 high for 30 $\mu$ s	OUT1, OUT2, OUT3 On
4	OUT1, OUT2, OUT3 On	1	1	1	0	All high for 190 ms	Power Good
5	Power Good	1	1	1	1	VIN2, VIN3, or VIN4 low for 30 $\mu$ s	OUT1, OUT2, OUT3 On

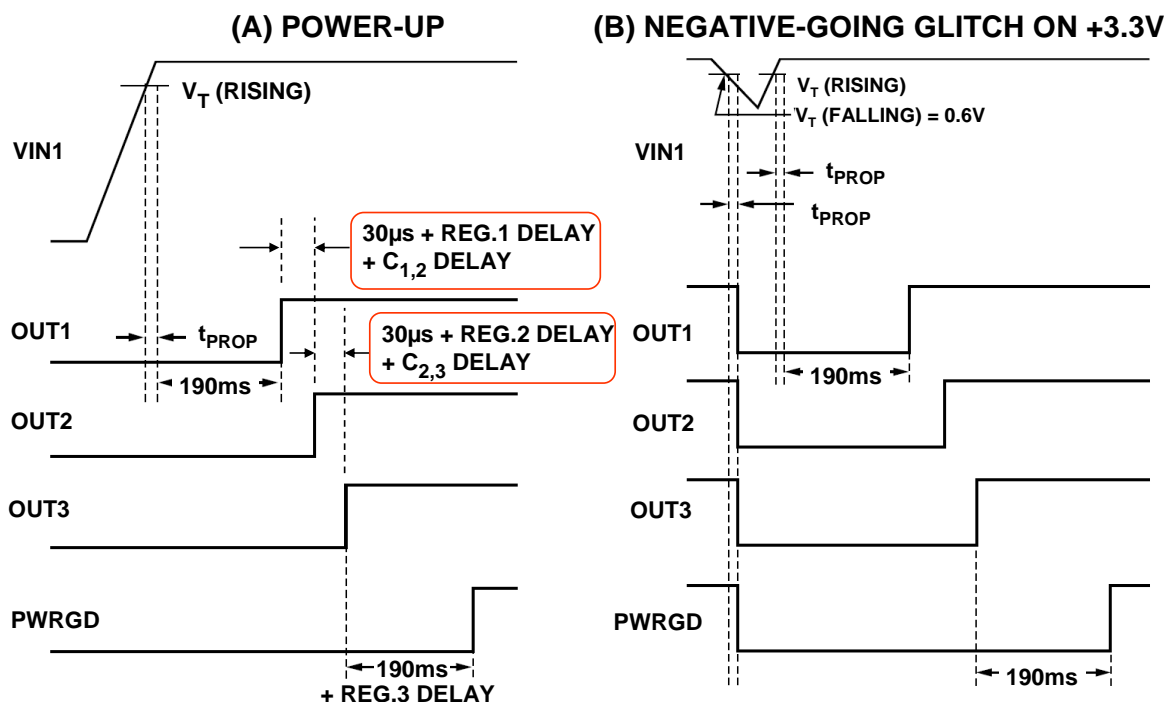
This shows a typical application of the ADM1185 monitoring four supplies and sequencing three regulators. The resistor dividers scale the monitored voltages to equal the 0.6 V internal comparator reference voltage. External capacitors can be added in order to add more delay between the enabling of the regulators.

OUT1 is an open-drain active high output. In this application, OUT1 is connected to the enable pin of Regulator 1. Before the voltage on VIN1 has reached 0.6 V, this output is switched to ground, disabling Regulator 1. Note that all outputs are driven to ground as long as there is at least 1 V on the  $V_{CC}$  pin of the ADM1185. When the main system voltage reaches 2.9 V, VIN1 detects 0.6 V. This causes OUT1 to assert after a 190 ms (typical) delay. When this occurs, the open-drain output switches high, and the external pull-up resistor pulls the voltage on the Regulator 1 enable pin above its turn-on threshold, turning on the output of Regulator 1. The assertion of OUT1 turns on Regulator 1. The 2.5 V output of this regulator begins to rise. This is detected by input VIN2. When VIN2 detects the 2.5 V rail rising above its UV point, it asserts output OUT2, which turns on Regulator 2. A capacitor can be placed on the VIN2 pin to slow the rise of the voltage on this pin. This effectively sets a time delay between the 2.5 V rail powering up and the next regulator enable. The same scheme is implemented with the other input and output pins. Every rail that is turned on via an output pin, OUTx, is monitored via an input pin VIN(x + 1).

The final comparator inside the VIN4 pin detects the final supply turning on, which is 1.2 V in this case. The output pins, OUT1 to OUT3, are logically AND'd together to generate a system power-good signal (PWRGD). There is an internal 190 ms delay (typical) associated with the assertion of the PWRGD output.

Note that the soft-start feature can be used if desired to control the output voltage ramp-up of any or all the regulators. Also, the regulators can be sequenced in any desired order by their placement in the chain with respect to OUT1, OUT2, and OUT3.

## Timing Diagram for ADM1185



This shows the timing diagram for power-up (A) and for a negative-going glitch on the +3.3 V line (B).

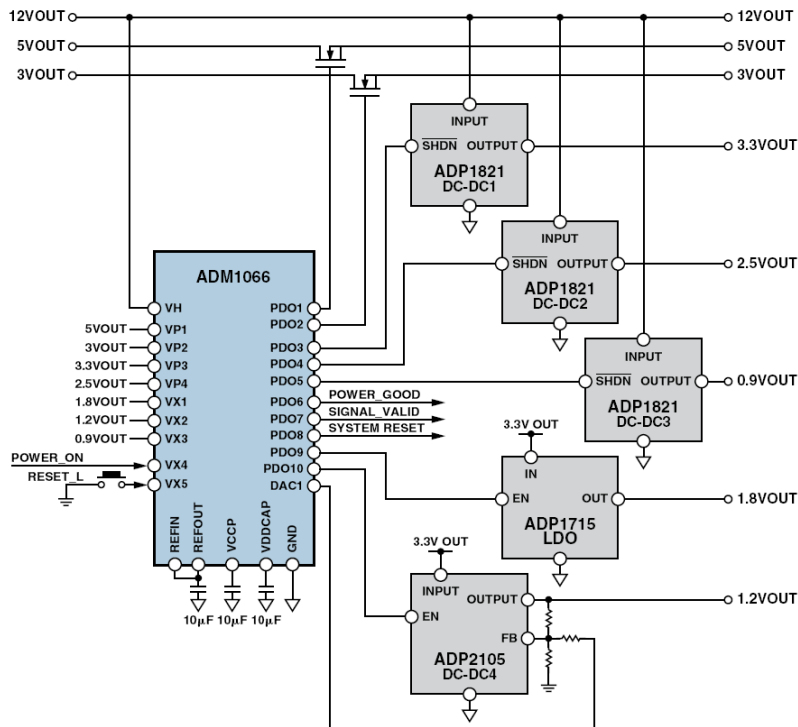
The operation in the power-up state has been explained on the previous page.

Once PWRGD is asserted, the logical core latches into a different mode of operation. During the initial power-up phase, each output directly depends on an input (for example, VIN3 asserting causes OUT3 to assert). When power-up is complete, this function is redundant.

Once in the PWRGD state, the following behavior can be observed:

- If the main 3.3 V supply monitored via VIN1 faults in the power-good state, the PWRGD output is deasserted to warn the downstream controller. All outputs (OUT1 to OUT3) are immediately turned off, disabling all locally generated supplies.
- If a supply monitored by VIN2 to VIN4 fails, the PWRGD output is deasserted to warn the controller, but the other outputs are not deasserted.

## ADM1066 Super Sequencer®

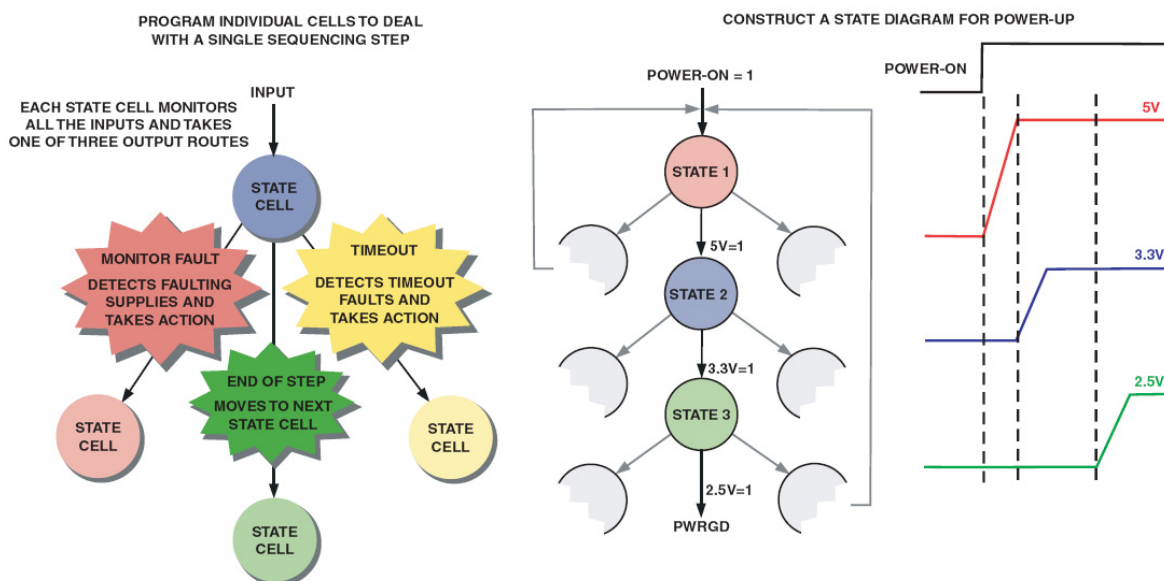


Sequencing more than three or four supply rails can become quite complex using individual sequencing ICs. Consider a system with eight voltage rails that requires a complex power-up sequence. Each rail must be monitored for undervoltage and overvoltage faults. In the event of a fault, all voltages could be turned off, or a power-down sequence could be initiated, depending on the failure mechanism. Actions must be taken depending upon the state of the control signals, and flags must be generated depending on the state of the power supplies. Implementing a circuit of this complexity with discrete devices and simple ICs may require hundreds of individual components, a huge amount of board space, and a significant combined cost. In systems with four or more voltages, it may make sense to use a centralized device to manage the power supplies. An example of this approach is shown above.

The ADM106x Super Sequencer family continues to use comparators, but with some important differences. Two comparators are dedicated to each input so that undervoltage and overvoltage detection can be implemented, thus providing windowed monitoring for the rails. An undervoltage fault is the normal condition of a rail before it powers up, so this indication is used for sequencing. An overvoltage condition usually indicates a critical fault—such as a shorted FET or inductor—and calls for immediate action.

Systems with higher supply counts usually have greater complexity, and thus have tighter accuracy constraints. Also, setting accurate thresholds with resistors becomes challenging at lower voltages, such as 1.0 V and 0.9 V. Although a 10% tolerance may be acceptable on a 5 V rail, this tolerance is generally insufficient on a 1 V rail. The ADM1066 allows input detector comparator thresholds to be set within 1% worst case, independent of the voltage (as low as 0.6 V)—and across the entire temperature range of the device. It adds internal glitch filtering and hysteresis to each comparator. Its logic inputs can be used to start the power-up sequence, shut down all rails, or perform other functions.

## State Machine Based Sequencing Engine Core

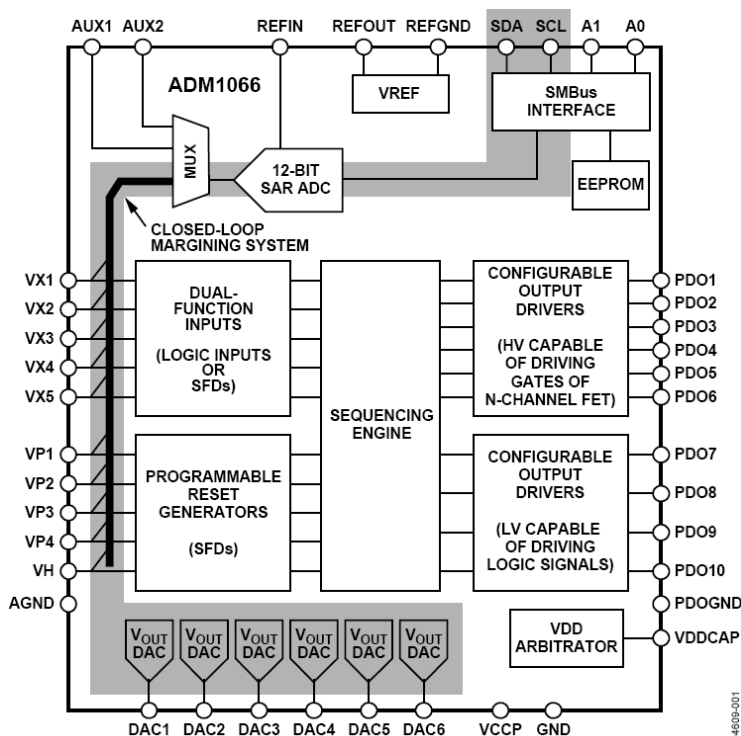


The information from the bank of comparators is then fed into a powerful and flexible state machine core and can be used for various purposes:

1. **Sequencing:** When the output voltage of a recently enabled supply comes into a window, a time delay can be triggered to turn on the next rail in the power-up sequence. Complex sequencing, with multiple power-up and power-down sequences, or vastly different sequences for power-up and power-down is possible.
2. **Timeout:** If a rail that has been enabled does not come on as expected, a suitable course of action can be taken (such as generating an interrupt or shutting down the system). A purely analog solution would simply hang at that point in the sequence.
3. **Monitoring:** If the voltage on any rail moves out of the preset window, a suitable course of action can be taken—depending on the rail that faulted, the type of fault that occurred, and the current operating mode. Systems with more than five supplies are often expensive, so comprehensive fault protection is crucial. An on-board charge pump is used to generate approximately 12 V of gate drive, even if the highest available system voltage is as low as 3 V, allowing outputs to directly drive series NMOS FETs. Additional outputs enable or shut down dc-to-dc converters or regulators, allowing an output to internally pull up to one of the inputs or the on-board regulated voltage. The outputs can also be asserted open-drain. Outputs may also be used as status signals such as power good or power-on reset. Status LEDs can be directly driven from the outputs if required.

The state machine core is programmed via the industry-standard 2-wire SMBus interface.

## ADM1066 Super Sequencer



The ADM1066 is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple-supply systems. In addition to these functions, the ADM1066 integrates a 12-bit ADC and six 8-bit voltage output DACs. These circuits can be used to implement a closed-loop margining system that enables supply adjustment by altering either the feedback node or reference of a dc-to-dc converter using the DAC outputs.

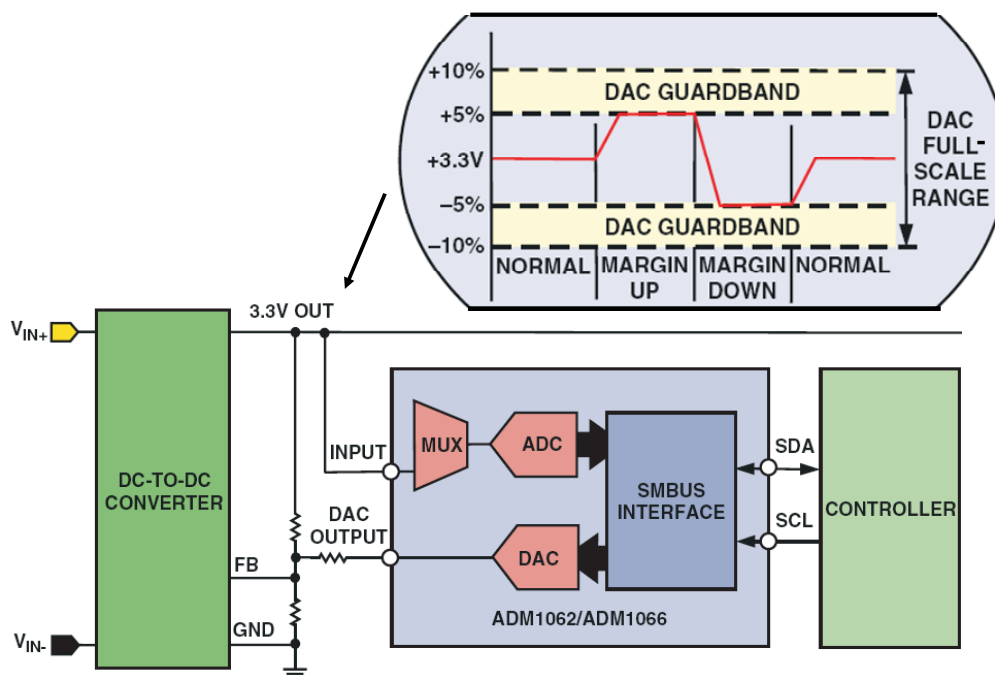
Supply margining can be performed with a minimum of external components. The margining loop can be used for in-circuit testing of a board during production (for example, to verify the board's functionality at  $-5\%$  of nominal supplies), or can be used dynamically to accurately control the output voltage of a dc-to-dc converter.

The device also provides up to 10 programmable inputs for monitoring under, over, or out-of-window faults on up to 10 supplies. In addition, 10 programmable outputs can be used as logic enables. Six of them can also provide up to a 12 V output for driving the gate of an NMOS FET, which can be placed in the path of a supply.

The logical core of the device is a sequencing engine. This state-machine-based construction provides up to 63 different states. This design enables very flexible sequencing of the outputs, based on the condition of the inputs.

The device is controlled via configuration data that can be programmed into an EEPROM. The whole configuration can be programmed using an intuitive GUI-based software package provided by Analog Devices, Inc. The on-board nonvolatile memory allows it to be reprogrammed as many times as necessary, while the sequencing and monitoring needs of the system evolve during the development process. This means that the hardware design can be completed early in the prototype process, and optimization of the monitoring and sequencing can be done as the project progresses.

## Closed-Loop Supply Margining Using ADM1062/ADM1066



In addition to monitoring multiple voltage rails and providing a solution for complex sequencing, integrated power management devices, such as the ADM1066, also provide the tools to temporarily or permanently adjust individual rail voltages. The voltage output of a dc-to-dc converter or regulator can be altered by adjusting the voltage at the trim or feedback node of that device. Typically, a resistive divider between the output and ground of the module sets a nominal voltage at the trim/feedback pin. This, in turn, sets a nominal output voltage. Simple schemes involving switching extra resistors or controlling variable resistances in the feedback loop will alter the trim/feedback voltage and hence adjust the output voltage.

The ADM1066 is equipped with digital-to-analog converters (DACs) to provide direct control over the trim/feedback node. For maximum efficiency, these DACs do not operate between ground and a maximum voltage; instead they operate across a relatively narrow window centered on the nominal trim/feedback level. The value of an attenuation resistor scales the incremental change in the output of the power module with each LSB change of the DAC. This open-loop adjustment provides margin-up and margin-down levels equivalent to those obtained by digital resistance switching in the reference circuit, and will adjust the output to a similar accuracy.

The ADM1066 also includes a 12-bit analog-to-digital converter (ADC) to measure the supply voltages, so a closed-loop supply adjustment scheme can be implemented. With a given DAC output setting, the voltage output of the power module is digitized by the ADC and compared with the target voltage in software. The DAC can then be adjusted to calibrate the voltage output as closely as possible to the target voltage. This closed-loop scheme provides a very accurate method for supply adjustment. With a closed-loop method, the accuracy of the external resistors is completely irrelevant.

# Hot Swap Controllers

[www.analog.com/hotswap](http://www.analog.com/hotswap)



## What is a Hot Swap Controller?

- ◆ **A Hot Swap Controller is a device which allows a removable circuit board to be removed or inserted into a live system without interrupting the system's power supply bus.**
- ◆ **Typical Backplane Bus Voltages:  $-48\text{V}$ ,  $+12\text{V}$ ,  $+5\text{V}$**



Hot swap controllers allow a circuit board to be removed or inserted into a live system without interrupting the system power supply bus.

They are useful in many critical infrastructure applications such as telecommunications systems, servers, switchers and routers, and base stations—virtually any system which uses high currents and must remain operational while repairs, upgrades, or modifications are made.

The standard backplane voltage for telecommunications is  $-48\text{ V}$ . This standard had its origins in the early days of the telephone network. The  $48\text{ V}$  supply was considered to be the largest dc voltage that was not lethal under normal circumstances, and was a standard voltage easily generated by a battery backup bank made up of four  $12\text{ V}$  batteries in series.

The negative voltage was chosen to minimize galvanic corrosion causing corrosion of cables under damp conditions. A conductor with a negative charge will repel chlorine ions, as  $\text{Cl}$  (chlorine) ions are negative also. If the conductor were to have a positive charge,  $\text{Cl}$  ions would be attracted. This form of corrosion protection is called cathodic protection. It is often used for pipelines, bridges, etc. Such protection was very important in the days of open wire transmission lines.

Other standard backplane voltages are  $+12\text{ V}$  and  $+5\text{ V}$ , and there are others.



## Hot Swap Techniques

- ◆ **Using short pin on connector**
  - **Provided delay on enabling Power Supply to eliminate arcing at connectors.**
- ◆ **RC / Slew control on Power Supply Switch**
  - **This allowed the voltage to increase slowly and hence charge capacitors slowly reducing inrush current spikes.**
- ◆ **Some problems that remained**
  - **No overcurrent protection**
  - **No true inrush current protection—current limited**
  - **No Short circuit protection**
- ◆ **Benefits of Integrated Hot Swap controllers**
  - **Closed Loop Accurate Current Control**
  - **True linear Soft Start control**
  - **Programmable timing circuit breaker**
  - **NMOS series-pass FETs**

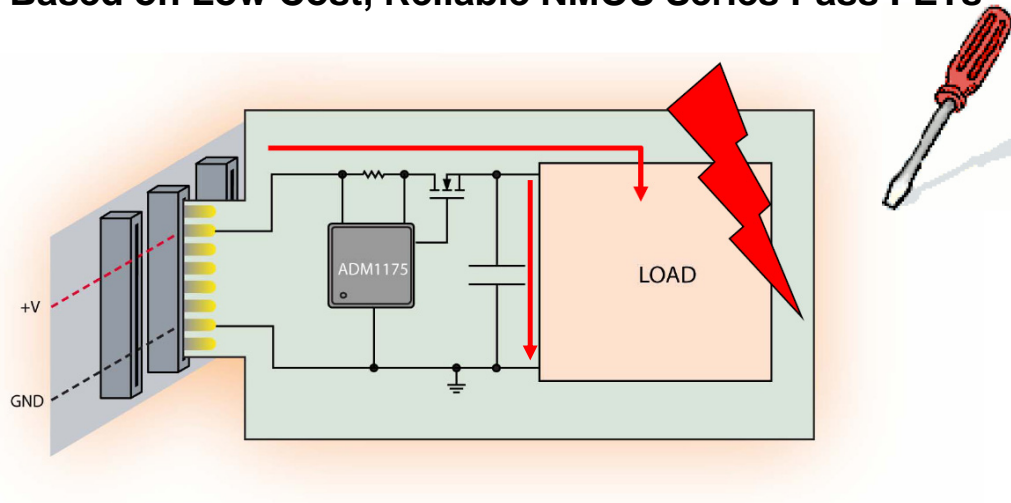
An early hot swap technique was to use a short pin on the connector for the power supply connection. This allowed all pins in the connector to be firmly in place before the actual power was applied, thereby minimizing arcing.

Other techniques were used, such as RC slew-rate limiting on the power supply switch, but modern ICs allow the function to be performed much more reliably and seamlessly.

Integrated hot swap controllers provide overcurrent protection, inrush current limiting, soft-start, and programmable timer controlled circuit breakers. The majority of IC hot swap controllers are designed to operate with low cost and highly reliable NMOS series pass FETs as the main power switching device.

## Functions of a Hot Swap Controller

- ◆ **Limits Inrush Current**
- ◆ **Provides Short Circuit protection**
- ◆ **Provides Active Current limiting**
- ◆ **Based on Low Cost, Reliable NMOS Series Pass FETs**



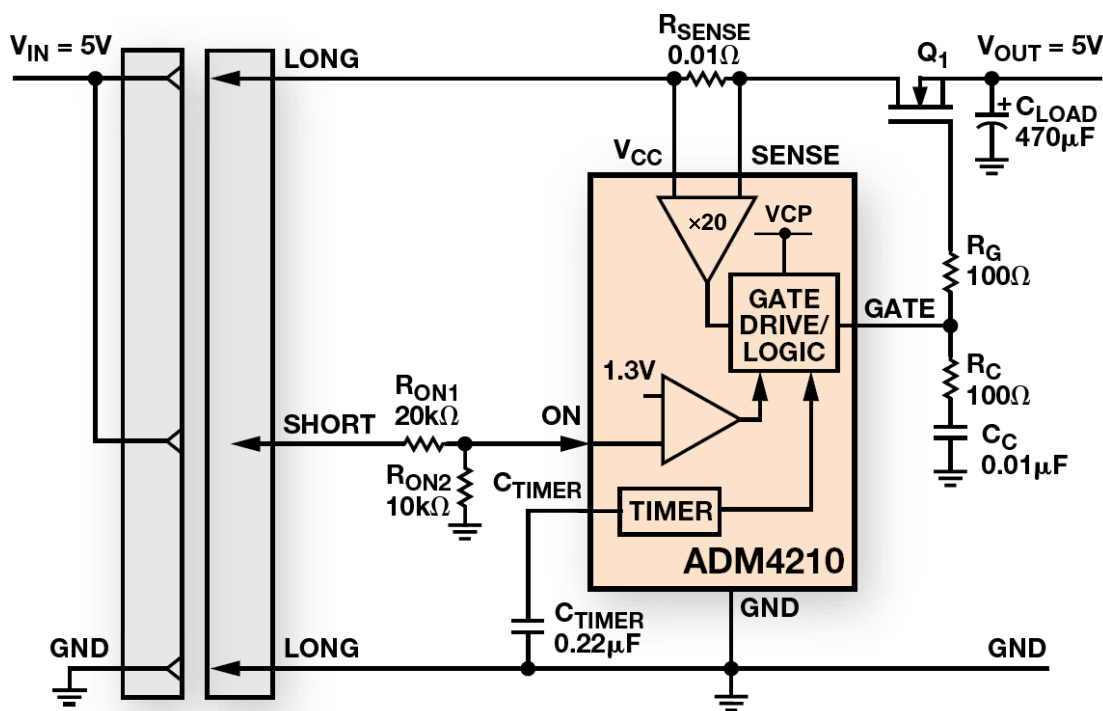
The basic functions of a hot swap controller are shown here. A primary function is to limit the inrush current when the card is inserted. The total inrush current can be quite high, since it is made up of not only the circuit current but also the initial current required to charge large bulk filter capacitors.

The hot swap controller must also provide short circuit protection as well as active current limiting.

The basic switch element chosen is almost always a low cost, reliable NMOS series pass FET as shown in the diagram.

The low output impedance of the NMOS FET source follower makes it relatively insensitive to bulk capacitor loads, and the control loop is fairly easy to stabilize. The gate drive signal to the NMOS FET must be several volts higher than the drain and source voltage, therefore charge pumps are often included in the hot swap controller IC to generate the required gate drive voltage. Although PMOS series pass devices do not require a separate supply for the gate drive, they have a higher output impedance, and the feedback loop is more difficult to stabilize. For this reason, the NMOS FET is the device of choice for the series pass element in a hot swap controller.

## Components of a Hot Swap Controller



This shows the basic components of a hot swap controller. The external components required are a sense resistor ( $R_{SENSE}$ ), NMOS FET switch, feedback compensation network ( $R_G$ ,  $R_C$ ,  $C_C$ ), voltage divider ( $R_{ON1}$ ,  $R_{ON2}$ ), and a timer capacitor ( $C_{TIMER}$ ).

The voltage divider sets the threshold voltage to the internal comparator in the hot swap controller IC. In the case of the ADM4210, the comparator reference voltage is 1.3 V. the divider network shown divides the 5 V bus voltage by a factor of 3. In this circuit, the threshold voltage referenced to the bus voltage is  $3 \times 1.3 V = 3.9 V$ .

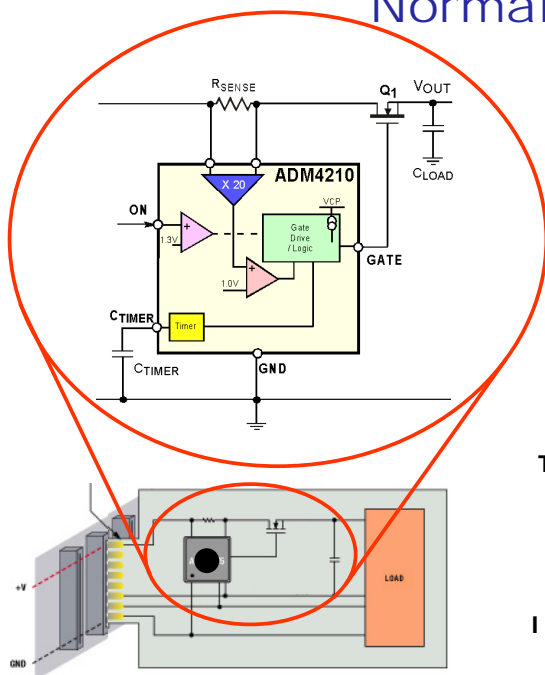
The internal circuit breaker is controlled by a current sense comparator which starts an overcurrent timeout sequence when the sense voltage is equal to 50 mV. The sense resistor limits the fault current to  $50 mV / R_{SENSE}$ . A sense resistor of  $0.01 \Omega$  gives a fault current of 5 A.

The timing control circuit gives an initial timing delay of  $273 ms/\mu F \times C_{TIMER}$  and a circuit breaker delay of  $22 ms/\mu F \times C_{TIMER}$ .

The timer generates ramp voltages by either sourcing or sinking current in or out of the  $C_{TIMER}$  capacitor. The gate drive is turned on or off by two additional comparators and control logic. The internal comparator threshold voltages are 0.2 V and 1.3 V.

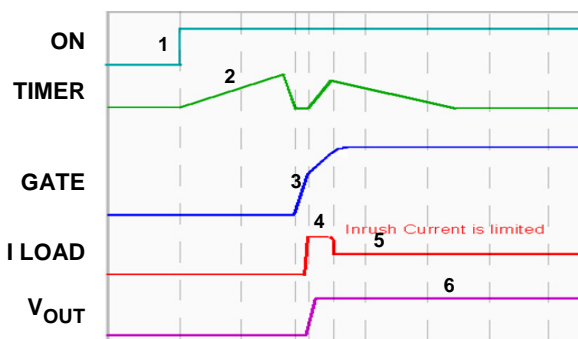
The ADM4210 also contains a gate drive circuit for the external NMOS FET using an internal charge pump. The gate driver consists of a 12  $\mu A$  pull-up current source from the internal charge pump voltage. The internal charge pump voltage range is typically 7.5 V to 11 V above  $V_{CC}$ , for  $V_{CC}$  between 3 V and 15 V.

## How the Hot Swap Controller Works for Normal Power Up



### Normal Power Up

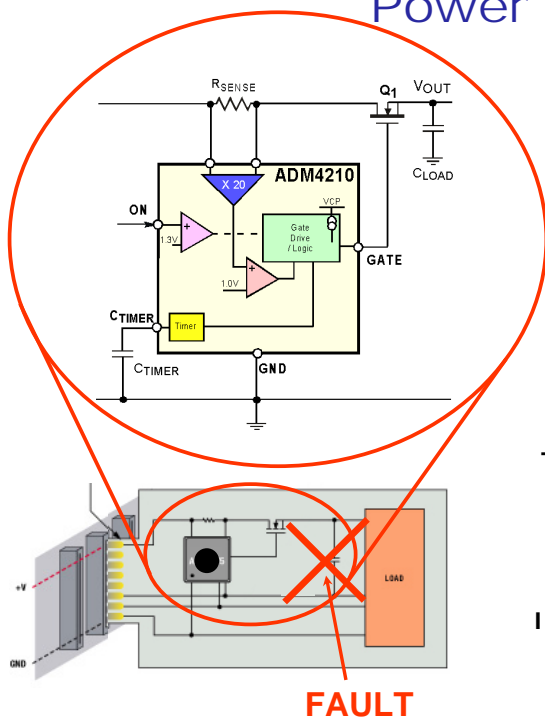
1. Controller is enabled
2. Timer Cycles Initial Period
3. Gate comes up
4. Inrush Current is Limited
5. Inrush Current falls off to normal
6. Power up complete



This figure shows how a typical hot swap controller works for normal power up conditions.

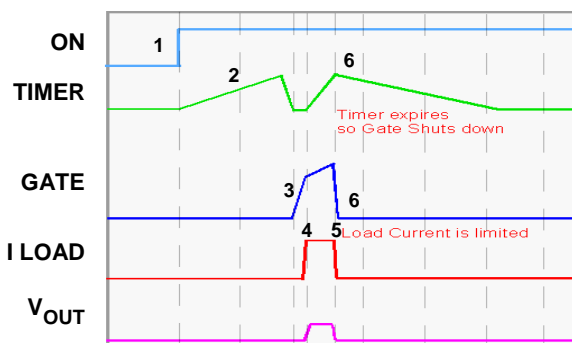
1. When the card is plugged in and the input voltage crosses the undervoltage lockout threshold, the controller is enabled, starting the internal timer.
2. The timer voltage ramps up at a rate controlled by the external  $C_{TIMER}$  capacitor and a pull-up current of  $5\ \mu\text{A}$ .
3. When the timer voltage reaches  $1.3\ \text{V}$ , this is the end of the first timing cycle. The timer current changes to a pull-down current of  $100\ \mu\text{A}$ , and the ramp voltage changes direction. When the ramp voltage reaches  $0.2\ \text{V}$ , the GATE pin is pulled high turning on the NMOS FET.
4. The second timer cycle is then enabled. When the voltage across the sense resistor exceeds the circuit breaker trip voltage, a timer pull-up current of  $60\ \mu\text{A}$  is activated.
5. If the sense voltage falls below the current limit level before the timer voltage reaches  $1.3\ \text{V}$ , the  $60\ \mu\text{A}$  pull-up is disabled and a  $2\ \mu\text{A}$  pull-down current is enabled. This is the normal operating mode if the overcurrent fault is only inrush current or a transient.
6. The  $2\ \mu\text{A}$  pull-down current causes the ramp voltage to return to zero, and the power-up cycle is completed.

## How the Hot Swap Controller Works for Power Up Into a Fault



### Power Up into a Fault

1. Controller is enabled
2. Timer Cycles Initial Period
3. Gate comes up
4. Inrush Current is Limited
5. Current remains at limit due to Fault
6. Timer Expires and FET is Shutdown



This figure shows how the hot swap controller works when a card having a short circuit is plugged in.

1. When the card is plugged in and the input voltage crosses the undervoltage lockout threshold, the controller is enabled, starting the internal timer.
2. The timer voltage ramps up at a rate controlled by the external C<sub>TIMER</sub> capacitor and a pull-up current of 5  $\mu$ A.
3. When the timer voltage reaches 1.3 V, this is the end of the first timing cycle. The timer current changes to a pull-down current of 100  $\mu$ A, and the ramp voltage changes direction. When the ramp voltage reaches 0.2 V, the GATE pin is pulled high turning on the NMOS FET.
4. The second timer cycle then enabled. When the voltage across the sense resistor exceeds the circuit breaker trip voltage, a timer pull-up current of 60  $\mu$ A is activated.
5. The short circuit continues, and the ramp voltage reaches the 1.3 V threshold. The short circuit timer has now expired.
6. The gate drive is pulled low, disabling the FET.

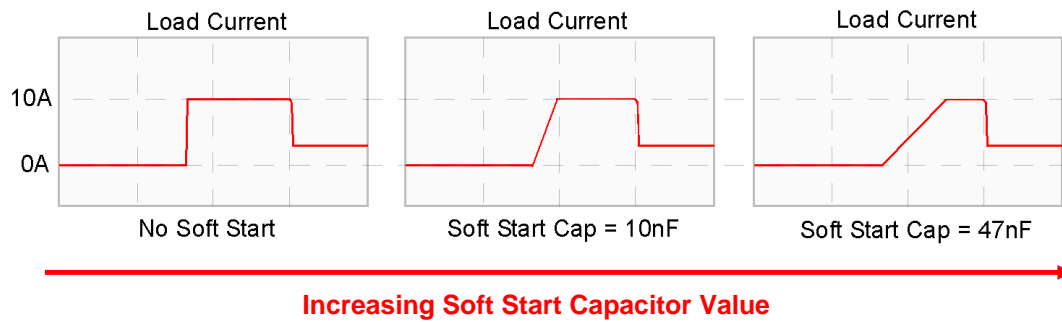
On the ADM4210-1, the timer function activates the 2  $\mu$ A pull-down once the 1.3 V threshold is reached, and continues to pull down until it reaches the 0.2 V threshold. At this point, the 100  $\mu$ A pull-down is activated, and the GATE pin is enabled. The device then keeps retrying.

The duty cycle of this automatic retry cycle is set to the ratio of 2  $\mu$ A/60  $\mu$ A, which approximates 3.8% on. The value of the timer capacitor determines the on-time of this cycle.

The ADM4210-2 model has a latch-off system whereby when a current fault is detected, the GATE is switched off after a time determined by the timer capacitor. Toggling the ON-CLR pin, or pulling the TIMER pin to GND for a brief period, resets this condition.

## Soft Start Gives Linear Inrush Current Control

- ◆ **Soft Start is a means by which Hot Swap controllers can control the inrush current increase to a safe level.**
- ◆ **If the nominal current limit was high (e.g. 10A), on start up, load capacitance may require all this current and more for a short period of time to charge up. This is inrush current.**
- ◆ **Even though the limit is maintained at 10A by the controller, the sudden jump from 0A to 10A can cause unwanted transients on the supply line.**
- ◆ **The effect of increasing soft start capacitor values on inrush current can be seen as follows:**



**Soft Start Available on ADM1170, ADM1171, ADM1177 and ADM1073 (–48V)**

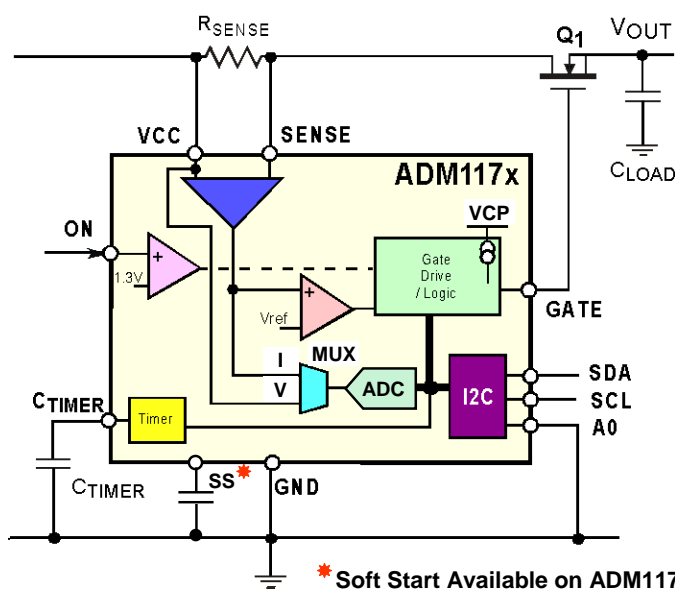
Soft start is a means by which a hot swap controller can control the inrush current to increase at a safe level. The function operates in a manner similar to the soft start feature found on many linear and switching regulators.

Because of large values of bulk capacitance, with no soft start feature, the hot swap controller current can jump from zero to the current limit value. This current, called inrush current, is required to charge the input capacitance and can create unwanted transients on the supply line.

As shown in this figure, the soft start feature slows down the rate of increase in charging current and reduces transient effects. Increasing the value of the soft start capacitor produces a proportional increase in the ramp-up time.

Many full-featured hot swap controllers such as the ADM1170, ADM1171, ADM1177, and ADM1073 have the soft start feature.

## Hot Swap Controller + Power Monitoring ADM1175, ADM1176, ADM1177, ADM1178



### Hot Swap Controller

1. Current Sense Comparator
2. Timer
3. ON Pin
4. FET Gate Driver

### + Power Monitoring

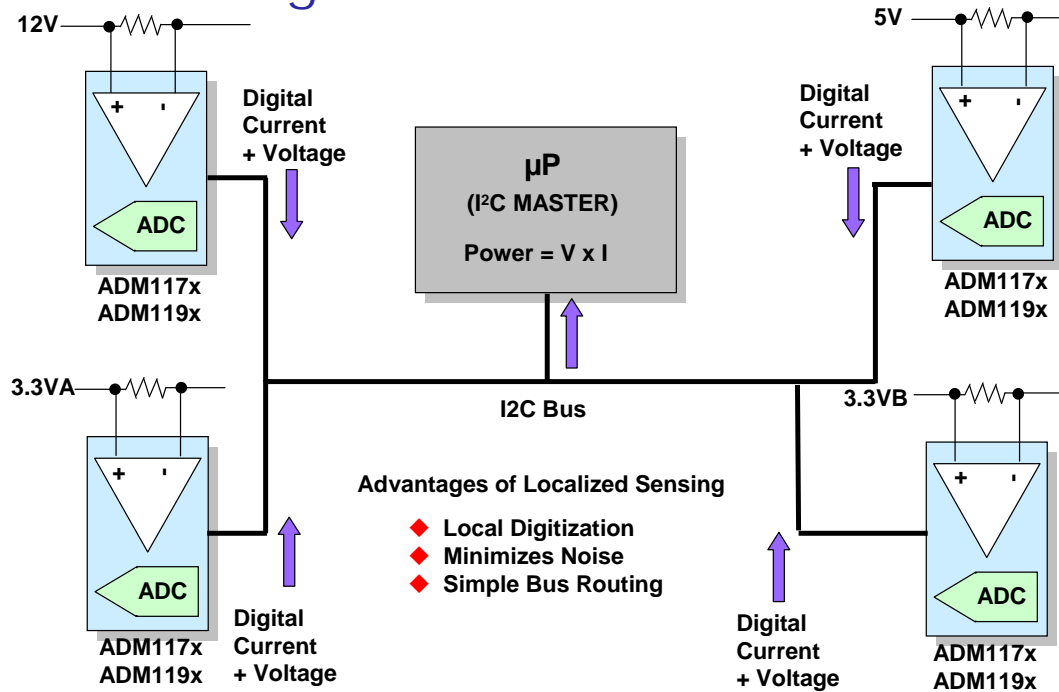
5.  $V_{CC}$  Voltage to MUX
6. CS AMP to MUX
7. 12-Bit ADC to I<sup>2</sup>C

The ADM1175/ADM1176/ADM1177/ADM1178-series are integrated hot swap controllers that have on-chip current sense comparator, time, ON function, and FET gate driver. Operation of these functions is similar to the ADM4210 previously described.

In addition, this family of devices offers digital current and voltage monitoring via an on-chip, 12-bit analog-to-digital converter (ADC), communicated through an I<sup>2</sup>C® interface.

A 12-bit ADC can measure the current seen in the sense resistor, as well as the supply voltage on the  $V_{CC}$  pin. An industry-standard I<sup>2</sup>C interface allows a controller to read current and voltage data from the ADC. Measurements can be initiated by an I<sup>2</sup>C command. Alternatively, the ADC can run continuously, and the user can read the latest conversion data whenever it is required.

## ADM117x/ADM119x Solution for Digital Power Measurement



As well as performing the hot swap function, the ADM1175/ADM1176/ADM1177/ADM1178-series can monitor total power consumed by each PC board via the on-chip ADC and the I²C bus.

Noise is minimized by performing the digitization locally on each PC board and transmitting the current and voltage measurements digitally, rather than transmitting the actual PC board voltages and the current-sense signals over system wiring.

The ADM1191 and ADM1192 perform the power monitoring function, but without the hot swap feature.



# Temperature Monitoring

[www.analog.com/temperature](http://www.analog.com/temperature)

## Types of Temperature Sensors

THERMOCOUPLE	RTD	THERMISTOR	SEMICONDUCTOR
<b>Widest Range:</b> –184°C to +2300°C	<b>Range:</b> –200°C to +850°C	<b>Range:</b> 0°C to +100°C	<b>Range:</b> –55°C to +150°C
<b>High Accuracy and Repeatability</b>	<b>Fair Linearity</b>	<b>Poor Linearity</b>	<b>Linearity: 1°C</b> <b>Accuracy: 1°C</b>
<b>Needs Cold Junction Compensation</b>	<b>Requires Excitation</b>	<b>Requires Excitation</b>	<b>Requires Excitation</b>
<b>Low-Voltage Output</b>	<b>Low Cost</b>	<b>High Sensitivity</b>	<b>10mV/K, 20mV/K, or 1μA/K Typical Output</b>

Measurement of temperature is critical in modern electronic devices, especially expensive computers with densely packed circuits which dissipate considerable power in the form of heat. Knowledge of system temperature can also be used to control battery charging as well as prevent damage to expensive microprocessors.

Compact high power portable equipment often has fan cooling to maintain junction temperatures at proper levels. In order to conserve battery life, the fan should only operate when necessary. Accurate control of the fan requires a knowledge of critical temperatures from the appropriate temperature sensor.

Accurate temperature measurements are required in many other measurement systems such as process control and instrumentation applications. In most cases, because of low-level nonlinear outputs, the sensor output must be properly conditioned and amplified before further processing can occur.

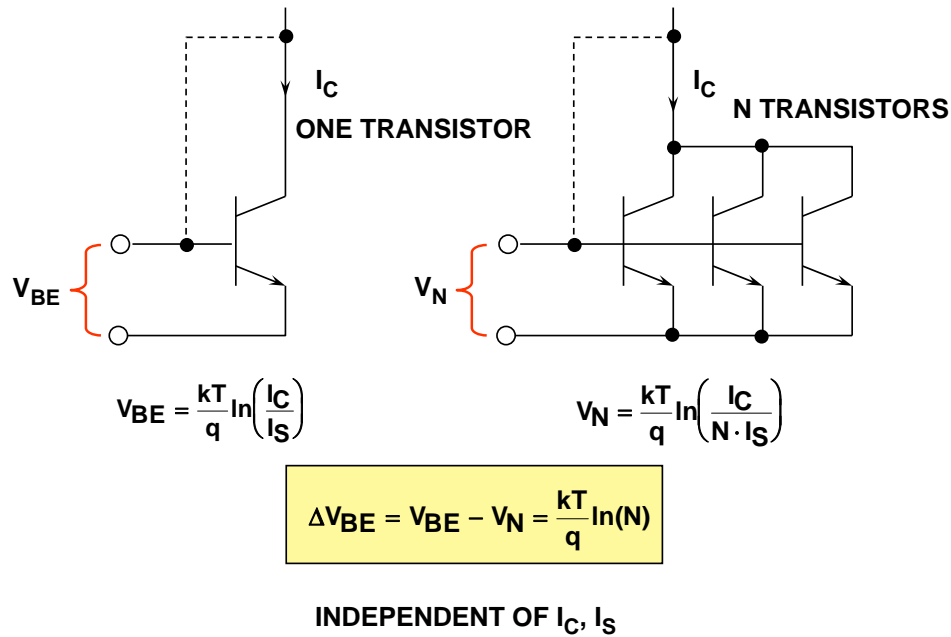
Thermocouples have the widest temperature range of all the sensors, but require specialized signal conditioning circuitry because of their low-level outputs and non-linear transfer functions

Resistance Temperature Devices (RTDs) are accurate, but require excitation current and are generally used in bridge circuits.

Thermistors have the most sensitivity but are the most non-linear. However, they are popular in portable applications such as measurement of battery temperature and other critical temperatures in a system.

Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about –55°C to +150°C. Internal amplifiers can scale the output to convenient values, such as 10 mV/°C. Semiconductor temperature sensors can be integrated into multi-function ICs which perform a number of other hardware monitoring functions, and are ideal for most system applications where temperature is critical.

## Basic Relationship for IC Temperature Sensors



Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ . All semiconductor temperature sensors make use of the relationship between a bipolar junction transistor's (BJT) base-emitter voltage to its collector current:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

where  $k$  is Boltzmann's constant,  $T$  is the absolute temperature (K),  $q$  is the charge of an electron, and  $I_S$  is a current related to the geometry and the temperature of the transistors. (The equation assumes a voltage of at least a few hundred mV on the collector, and ignores Early effects.)

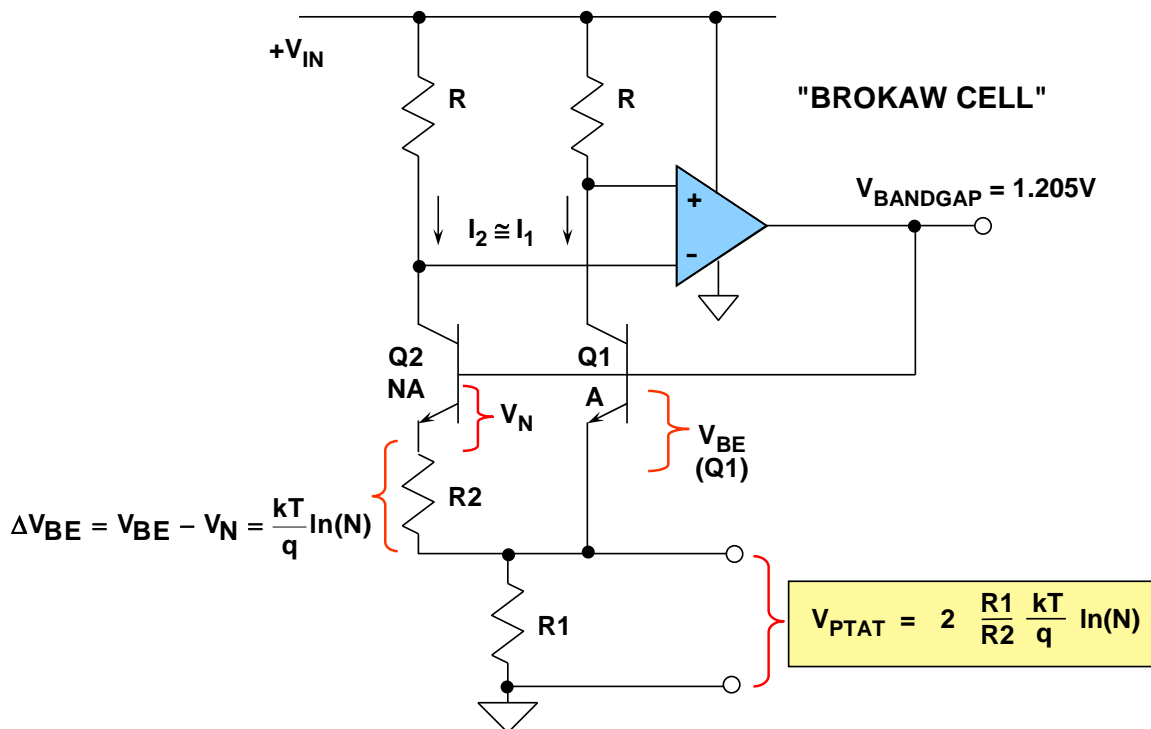
If we take  $N$  transistors identical to the first and allow the total current  $I_C$  to be shared equally among them, we find that the new base-emitter voltage is given by the equation

$$V_N = \frac{kT}{q} \ln\left(\frac{I_C}{N \cdot I_S}\right)$$

Neither of these circuits is of much use by itself because of the strongly temperature dependent current  $I_S$ , but if we have equal currents in one BJT and  $N$  similar BJTs then the expression for the difference between the two base-emitter voltages is proportional to absolute temperature and does not contain  $I_S$ :

$$V_{BE} - V_N = \frac{kT}{q} \ln\left[\frac{\left(\frac{I_C}{I_S}\right)}{\left(\frac{I_C}{N \cdot I_S}\right)}\right] = \frac{kT}{q} \ln(N)$$

## Classic Band Gap Temperature Sensor

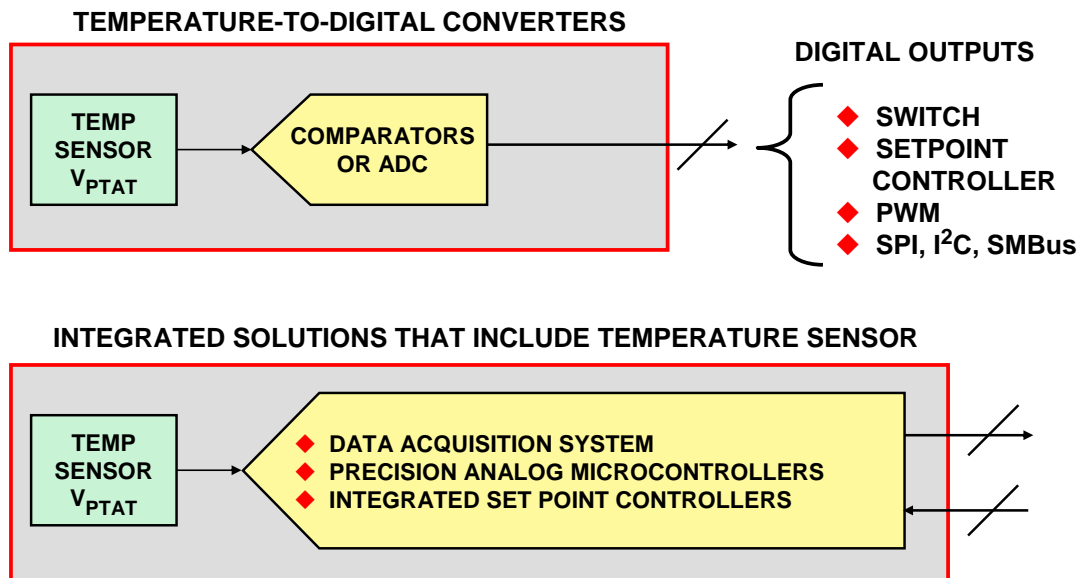


The circuit shown in this figure implements the previous equation and is known as the "Brokaw Cell". The voltage  $V_{\text{BE}} - V_{\text{N}}$  appears across resistor R2. The emitter current in Q2 is therefore  $(V_{\text{BE}} - V_{\text{N}})/R2$ . The op amp's servo loop and the resistors, R, force the same current to flow through Q1. The Q1 and Q2 currents are equal and are summed and flow into resistor R1. The corresponding voltage developed across R1 is proportional to absolute temperature (PTAT) and given by:

$$V_{\text{PTAT}} = \frac{2R1(V_{\text{BE}} - V_{\text{N}})}{R2} = 2 \frac{R1}{R2} \frac{kT}{q} \ln(N)$$

The band gap cell reference voltage,  $V_{\text{BANDGAP}}$ , appears at the base of Q1 and is the sum of  $V_{\text{BE}(Q1)}$  and  $V_{\text{PTAT}}$ .  $V_{\text{BE}(Q1)}$  is complementary to absolute temperature (CTAT), and summing it with  $V_{\text{PTAT}}$  causes the band gap voltage to be constant with respect to temperature (assuming proper choice of R1/R2 ratio and N to make the band gap voltage equal to 1.205 V). This circuit is the basic band gap temperature sensor, and is widely used in semiconductor temperature sensors.

## Analog Temperature Sensors are Now Integrated into Many Different Parts

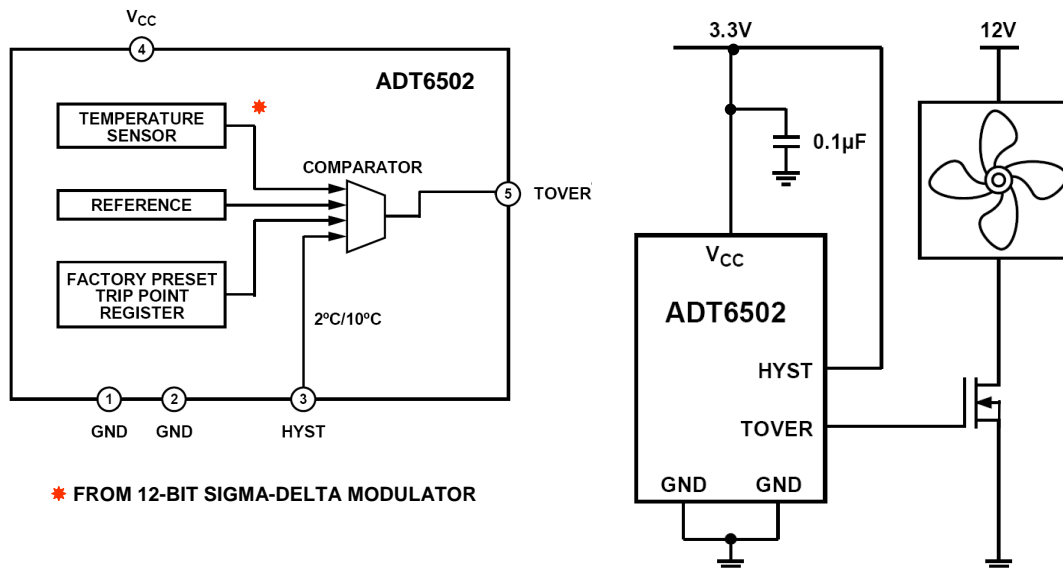


Voltage references form an integral part of data acquisition systems of all types. The  $V_{PTAT}$  voltage is conveniently part of the reference and is available for temperature sensing as well.

It is therefore relatively easy to integrate a temperature sensor into most modern ICs if one is required. The sensor monitors the temperature of its junction, which should be approximately equal to the ambient temperature, provided the total internal power dissipation of the device is low, and self-heating is not an issue.

Digital temperature sensors can take many forms. The simplest is a  $V_{PTAT}$  generator followed by a comparator which acts as a simple on/off function, depending on the comparator voltage reference. This type of temperature sensor forms the basis of modern setpoint controllers. More sophisticated digital temperature sensors use an ADC to convert the temperature sensor voltage into either a PWM signal, or bus-compatible digital signal.

## Low Cost, 2.7V to 5.5V, Micropower Temperature Switches in SOT-23



The ADT6501/ADT6502/ADT6503/ADT6504 are trip point temperature switches available in a 5-lead SOT-23 package. Each part contains an internal band gap temperature sensor for local temperature sensing. The band gap output voltage ( $V_{PTAT}$ ) is digitized with a 12-bit sigma-delta modulator.

The 12-bit output from the modulator is input into a digital comparator where it is compared with a factory set trip level. The output trip pin is activated if the temperature measured is greater than the factory set trip level. Overall accuracy for the ADT650x family is  $\pm 6^{\circ}\text{C}$  from  $-45^{\circ}\text{C}$  to  $+115^{\circ}\text{C}$ .

Factory set trip levels are available in  $10^{\circ}\text{C}$  increments from  $+35^{\circ}\text{C}$  to  $+115^{\circ}\text{C}$  for the ADT6501/ADT6502 and from  $-45^{\circ}\text{C}$  to  $+15^{\circ}\text{C}$  for the ADT6503/ADT6504.

The ADT6501/ADT6503 logic output is active low and open-drain. The ADT6502/ADT6504 logic output is active high and push-pull. The temperature is digitized to a resolution of  $0.0625^{\circ}\text{C}$  (12 bit). The factory settings are  $10^{\circ}\text{C}$  apart starting from  $-45^{\circ}\text{C}$  to  $+15^{\circ}\text{C}$  for the cold threshold models and from  $+35^{\circ}\text{C}$  to  $+115^{\circ}\text{C}$  for the hot threshold models.

These devices require no external components and typically consume  $30\text{ }\mu\text{A}$  supply current. Hysteresis is pin-selectable at  $2^{\circ}\text{C}$  and  $10^{\circ}\text{C}$ . The temperature switch is specified to operate over the supply range of  $2.7\text{ V}$  to  $5.5\text{ V}$ .

The ADT6501 and ADT6502 are used for monitoring temperatures from  $+35^{\circ}\text{C}$  to  $+115^{\circ}\text{C}$  only. Therefore, the logic output pin becomes active when the temperature goes higher than the selected trip point temperature.

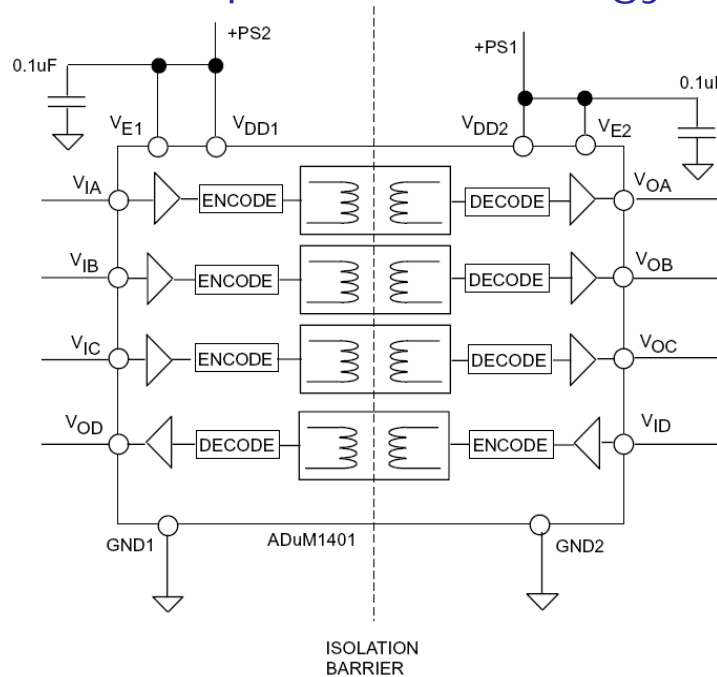
The ADT6503 and ADT6504 are used for monitoring temperatures from  $-45^{\circ}\text{C}$  to  $+15^{\circ}\text{C}$  only. Therefore, the logic output pin becomes active when the temperature goes lower than the selected trip point temperature.

The circuit shown uses the ADT6502 and an external NMOS FET to drive a fan. The output of the ADT6502 goes high when the temperature goes higher than the selected trip point temperature, turning on the FET and the fan.

## Digital Isolation and Isolated Power

[www.analog.com/icoupler](http://www.analog.com/icoupler)

## Digital Isolators Based on *iCoupler*® Technology



Digital isolators are extremely useful in separating system grounds. Designed primarily for galvanic isolation in industrial applications, the *iCoupler* isolator can be used to pass signals between ground planes at different potentials. No currents will circulate through the various grounds, since we are using transformers to isolate the grounds. The transfer rate through the *iCoupler* can be as high as 100 Mbps.

The ADuM140x1 are 4-channel digital isolators based on Analog Devices, Inc. *iCoupler* technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

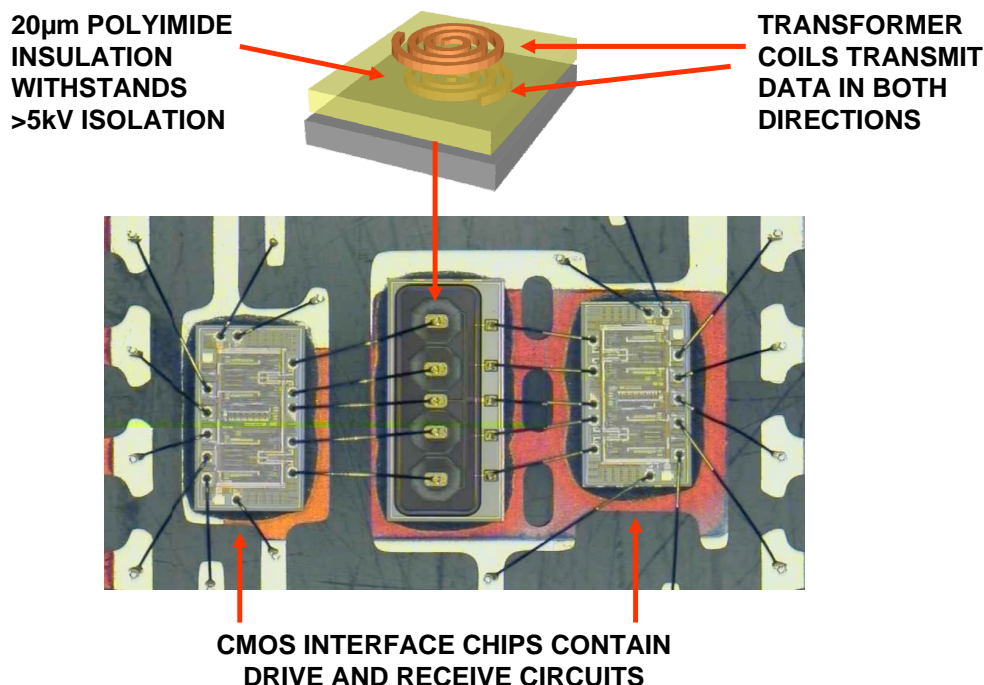
By avoiding the use of LEDs and photodiodes, *iCoupler* devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *iCoupler* digital interfaces and stable performance characteristics.

The need for external drivers and other discrete components is eliminated with these *iCoupler* products. Furthermore, *iCoupler* devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates and are more cost effective.

The ADuM140x isolators provide four independent isolation channels in a variety of channel configurations and data rates. All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. Unlike other optocoupler alternatives, the ADuM140x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.



## Construction of the *i*Coupler Digital Isolator

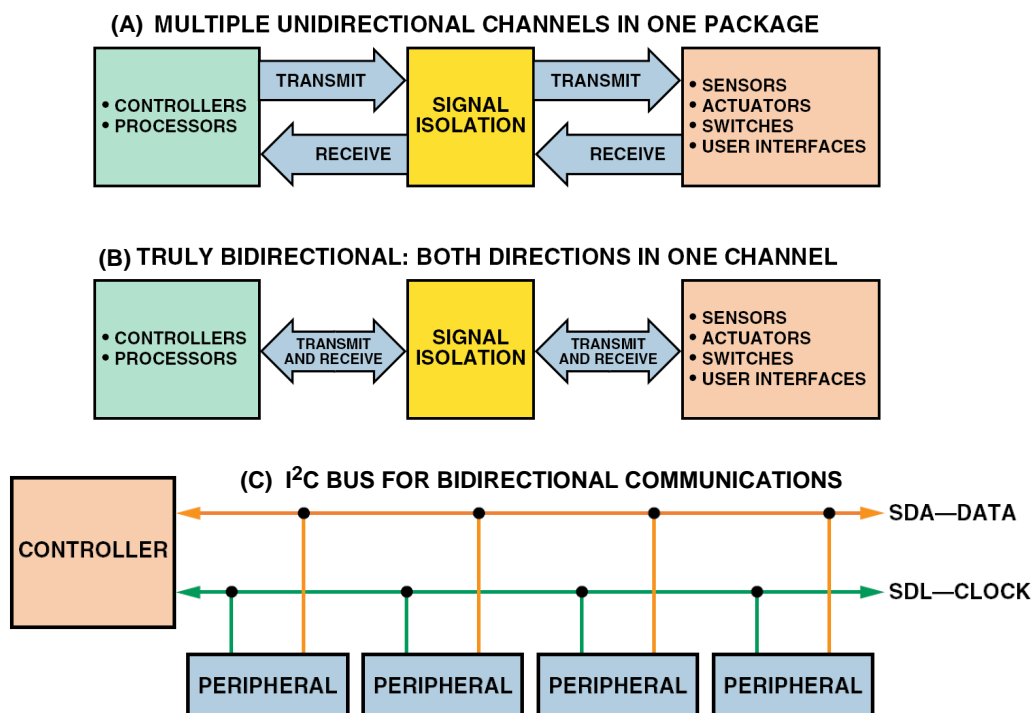


This photo shows a 4-channel digital isolator, which houses three die in a single package. Two CMOS interface circuits (left and right) integrate drive and receive electronics. The middle die contains four chip-scale microtransformers, each comprising metal (AlCu and Au) coils on either side of a 20 μm polyimide insulation layer. The polyimide is capable of withstanding more than 5 kV rms for one minute.

In most applications that require isolated data transmission, isolated power must be available on both sides of the isolation barrier, or it must be provided separately. System designers typically introduce isolated power by designing an isolated power supply using discrete components—including a transformer with the appropriate isolation rating—or by purchasing a commercial off-the-shelf isolated dc-to-dc converter. Each approach has its advantages and disadvantages. In the first instance, isolated power supplies may be custom tailored to an application, allowing system designers to optimize their cost, isolation rating, power output, or other important specifications depending on the application requirements. The downside, however, is that custom solutions tend to be bulky, require safety certification, and can lengthen development times. Commercially available isolated power supplies, on the other hand, can reduce time to market, but they carry a price penalty and may not be optimized to fit a particular application. While smaller in size than their custom counterparts, they are still fairly bulky, with only limited availability of surface-mount package options.

A third way is *isoPower*®, which combines the benefits of both options. *i*Coupler digital isolators condition and drive data across the transformers. *isoPower* uses the same chip-scale microtransformer technology, but instead of transmitting only data, *isoPower* employs switches, rectifiers, and regulators to generate power that is isolated to the same degree as the data channels.

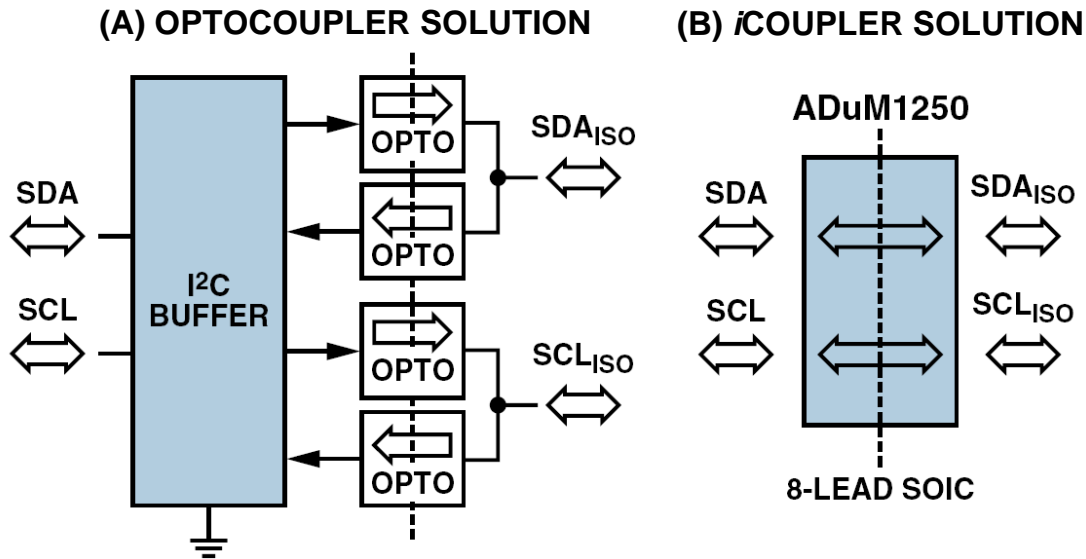
## Unidirectional and Bidirectional Transmission



In isolation, the term *bidirectional* has traditionally referred to an isolator with separate *transmit* and *receive* channels in one package—the isolator as a whole is capable of bidirectional data transfer, but the individual channels are unidirectional as shown in (A). This approach is compatible with communications protocols such as RS-232, RS-485, and SPI, but it is not compatible with true bidirectional communication protocols, such as I<sup>2</sup>C, SMBus, and PMBus, which support bidirectional data transfer through a single channel as shown in (B).

The inter-integrated-circuit (I<sup>2</sup>C) bus is a popular 2-wire, bidirectional communication protocol that was developed to provide simple, low-cost, short-distance communication between an on-board controller and its peripherals. I<sup>2</sup>C buses limit the cost of applications in which multiple devices share a single bus with a host controller, as shown in (C). Two bidirectional wires—one for the data and one for the clock—are used to achieve low cost at the expense of data rate, so I<sup>2</sup>C is typically used in systems with many peripherals running at data rates less than 1 Mbps. Systems that use a limited number of peripherals running at higher data rates will often employ protocols such as SPI.

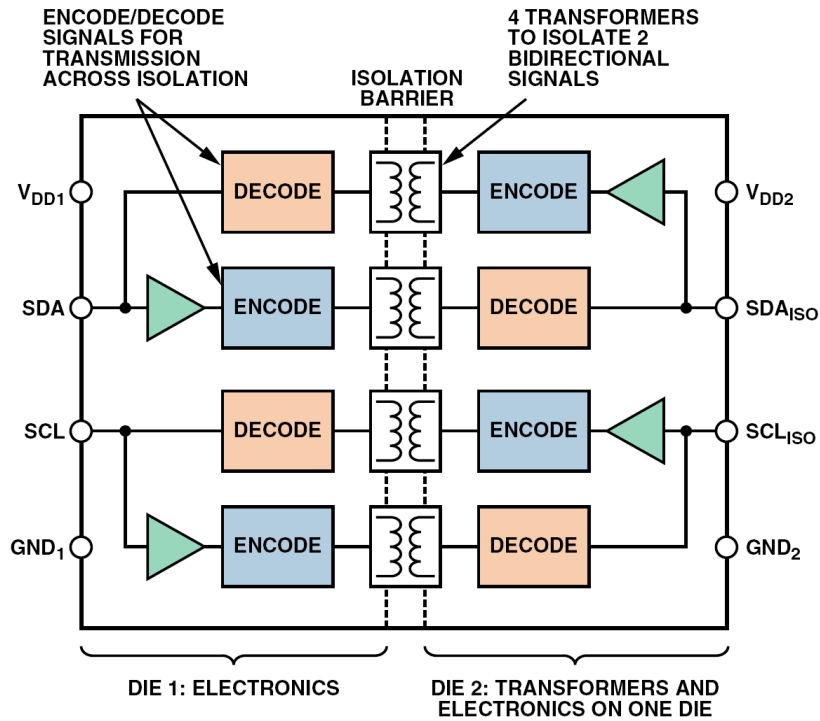
## *i*Coupler Simplifies True Bidirectional Isolation



The I<sup>2</sup>C isolation challenge has been that optocouplers are based on diodes that can transmit in only one direction, and are therefore inherently unidirectional. A bidirectional I<sup>2</sup>C bus could be isolated using optocouplers as shown in (A), but the implementation is messy. A special buffer is used to separate each bidirectional channel into two distinct channels: transmit and receive. Once separated, the four unidirectional channels can be individually isolated and then recombined. This solution requires four isolators and expands the bus from two wires to four wires. Additional circuitry is also required, making this solution costly and large, and defeating the original purpose of the 2-wire bus implementation: to save money and space.

The good news is that by adopting the new digital isolation techniques the circuitry that is used to separate, isolate, and recombine the data channels can be integrated into a single package. This approach can be implemented with the new ADuM1250 and ADuM1251 hot-swappable dual I<sup>2</sup>C isolators. Figure (B) illustrates how much more compact the *i*Coupler solution is.

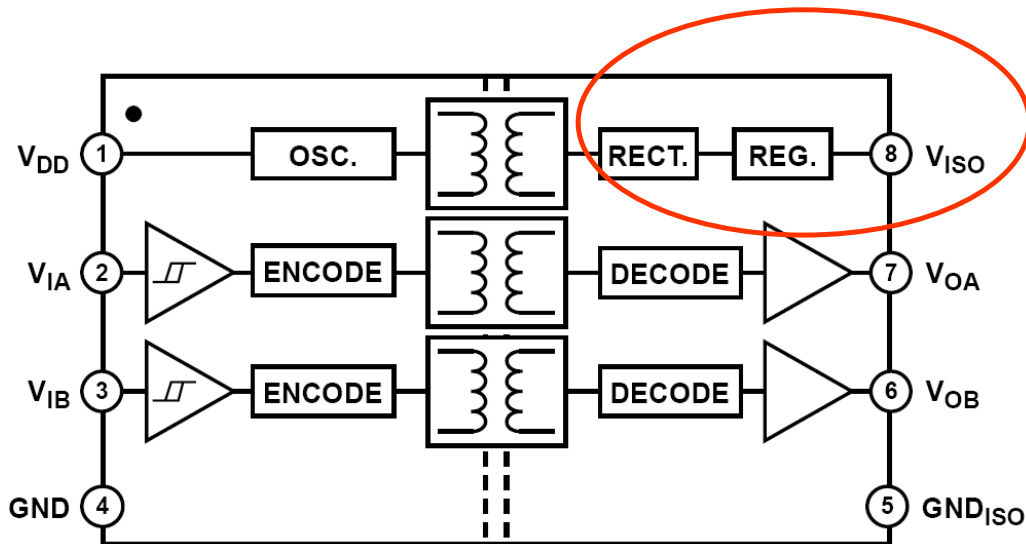
## True Bidirectional Isolation Using the ADuM1250 Digital Isolator



This figure shows how bidirectional isolation is achieved within the package. Just as the discrete solution employs a buffer to separate the two bidirectional channels into four unidirectional channels and four isolators, so, too, does the ADuM125x family. The difference is that all the electronics are integrated onto a single IC. A designer sees only the 2-wire interface, and the entire device is less than 40 mm<sup>2</sup>, a 90% reduction compared with the optocoupler/buffer solution, which takes up about 350 mm<sup>2</sup>.

The ADuM125x family operates at rates up to 1 MHz.

## ADuM5240 Dual-Channel Isolator with *isoPower* Integrated DC-to-DC Converter



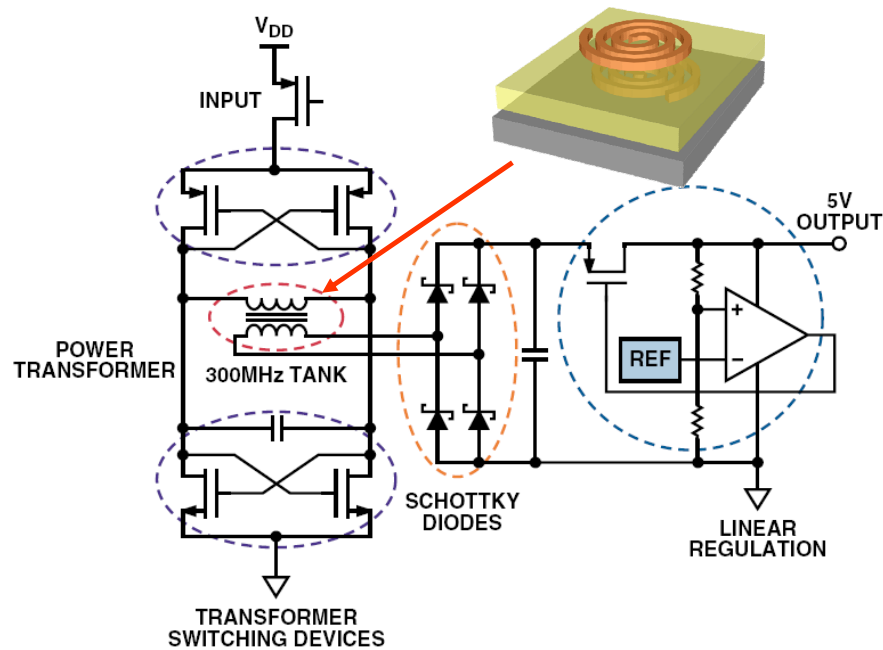
In addition to digital isolation, the capability of providing isolated power is important in many applications.

The ADuM524x are dual-channel digital isolators with *isoPower* integrated, isolated power. An on-chip dc-to-dc converter provides up to 50 mW of regulated, isolated power at 5 V, which eliminates the need for a separate isolated dc-to-dc converter in low power isolated designs.

The ADuM524x isolators provide two independent isolation channels in a variety of channel configurations, operating from a 5 V input supply. ADuM524x units may be used in combination with other *iCoupler* products to achieve greater channel counts.

The ADuM524x family of isolators operates at data rates up to 1 Mbps.

## *isoPower* Digital Isolator Implements Isolated Power



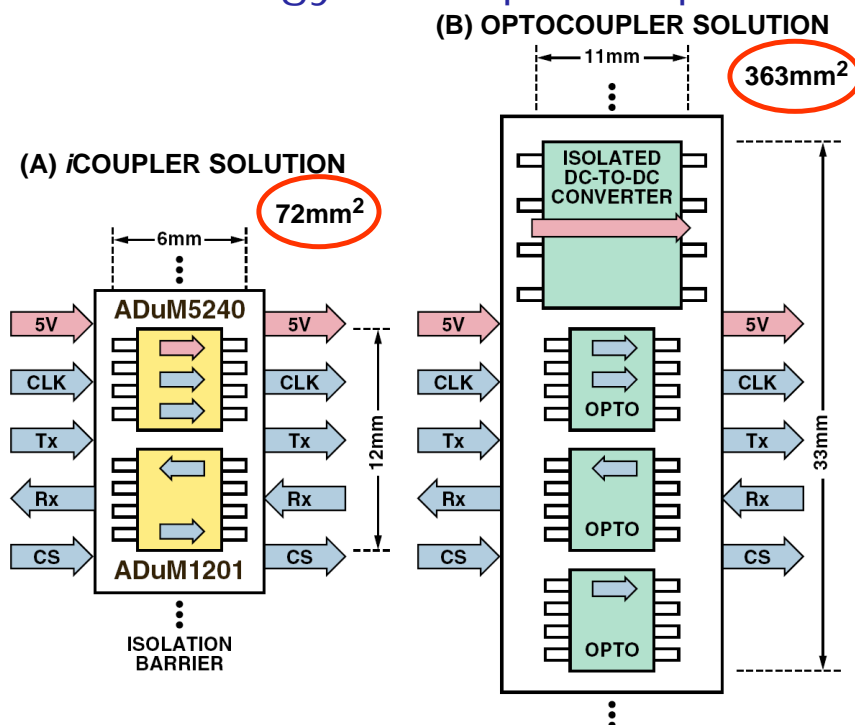
This figure shows the isolated power section of the ADuM5240, ADuM5241, and ADuM5242 the first *iCoupler* products with *isoPower*. Four cross-coupled CMOS switches generate an ac waveform that drives the transformer.

On the isolated side, Schottky diodes rectify the ac signal. The rectified signal is passed to a linear regulator, which maintains the output voltage at a nominal 5 V setpoint. The output is capable of supplying 10 mA of current.

The chip-scale microtransformers are made from 6  $\mu\text{m}$  thick gold, separated by a 20  $\mu\text{m}$  polyimide insulation layer, which is capable of providing greater than 5 kV rms isolation. Because the transformer coils, only 600 nm in diameter, have a low L/R ratio compared with conventional transformers, high-efficiency power generation requires high-frequency switching—on the order of 300 MHz.

As noted earlier, the transformers used to generate power employ the same process as those used to isolate data. The only significant difference between data and power channels is the conditioning circuitry on either side of the isolation barrier.

## Isolated SPI Interface Using *iCoupler* Technology and Optocouplers

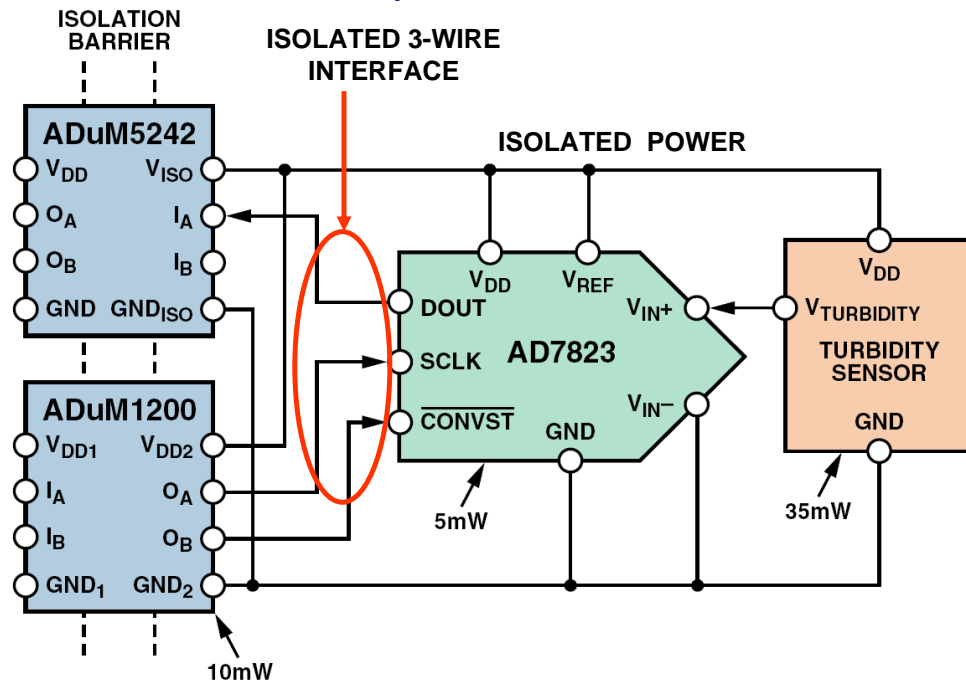


Combining data and power in a single, small, surface-mountable package, the ADuM524x family provides significant size and cost savings.

This figure shows typical physical configurations for isolated SPI interfaces. The *iCoupler* and *isoPower* solution (A) uses an ADuM5240 and an ADuM1201 to provide four channels of isolated data and up to 50 mW of isolated power, enough to power an ADC and a remote sensor. It is more compact and less expensive than the traditional approach using three optocouplers and an isolated dc-to-dc converter (B).

A third solution, using discrete transformers and other components, would consume even more area. Other combinations of ADuM524x *isoPower* and ADuM120x *iCoupler* products are possible, as are combinations of ADuM524x and most other *iCoupler* products.

## Completely Isolated Turbidity Sensor and ADC



This figure shows a completely isolated turbidity sensor system that measures the amount of particulates in a liquid solution and can be used to determine the cleanliness of a volume of water. They are increasingly being used in home appliances, such as dishwashers and washing machines, both to conserve water and to improve cleaning performance. Conventional appliances wash or rinse for a set time, overestimating the required level of cleaning to ensure that the load is fully clean at the end of the cycle. A turbidity sensor, however, can let the system know when to stop cleaning. The machine will use the optimal amount of water for the optimal time, thus minimizing waste while maximizing useful cleaning performance.

Because turbidity sensors must be immersed in the water, they present two challenges to an appliance designer. First, the sensor must be small enough to fit unobtrusively anywhere within the space where clothes or dishes are to be placed. The size of the sensor is, therefore, critical. Second, the powered circuit is immersed in water, so the sensor must be safely isolated from the rest of the system. If the physical insulation should fail, the user and the system electronics must not be harmed, and there must be no possibility of fire. Both the power and the data must therefore be isolated.

This figure demonstrates a cost-effective solution. The AD7823 low-power 8-bit 200 kSPS SAR ADC uses a 3-wire interface to convert the analog output of a turbidity sensor. The digitized turbidity data is transmitted across the galvanic isolation barrier of the ADuM1200 and ADuM5242. The 50 mW of isolated power from the ADuM5242 is sufficient to supply the ADuM1200, the AD7823, and the turbidity sensor. The combined area of the isolators and converter is less than 100 mm<sup>2</sup>, excluding external components.



## Digital Power Applications

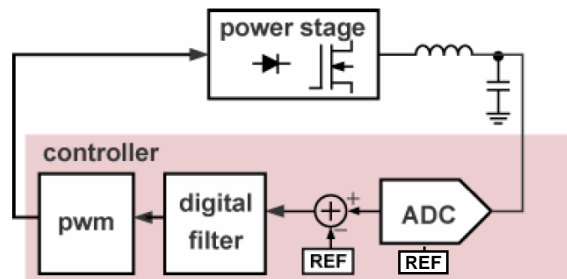
## Digital Power Management and Digital Power Control

### ◆ Digital Power Management

- Voltage Monitoring
- Sequencing
- Margining
- Temperature Monitoring and Fan Control
- Supervision
- Communication via data bus (SMBus, I<sup>2</sup>C, PMBus)

### ◆ Digital Power Control

- Real-time control of a power converter using an ADC and digital techniques within a feedback loop



We have seen how digital techniques are currently being used in voltage monitoring, sequencing, margining, temperature monitoring, fan control supervision, etc. These applications fall into the broad area loosely defined as digital power *management*. Although the results obtained through digital techniques (generally comparators or ADCs) may be used to control various system parameters, there is no real-time feedback loop in the classic sense of feedback control systems (operational amplifiers, servo systems, process control, etc.).

Digital power *control*, on the other hand, refers specifically to the real-time control of a power converter (ac-to-dc or dc-to-dc) using an ADC and digital techniques (digital filter, for example) within a feedback loop as shown above. As is usually the case, the digital approach offers many advantages (neglecting the economic factor for the moment).

Currently most point-of-load switching converters use analog techniques to control output voltage. There is no technical reason why the digital techniques illustrated above can't be used. The slow migration to digital power control is mostly due to economic factors. The digital implementation is simply more costly using today's CMOS process technology.

Digital control is, however, beginning to appear in the high power primary-side ac-to-dc converters and in secondary-sided dc-to-dc converters, where the requirements and economics make digital control an attractive alternative to traditional analog techniques.

As digital processes continue to shrink (analog processes do too, but not as rapidly), digital control will eventually progress further downstream in the power chain.

## Digital Control Loop Features

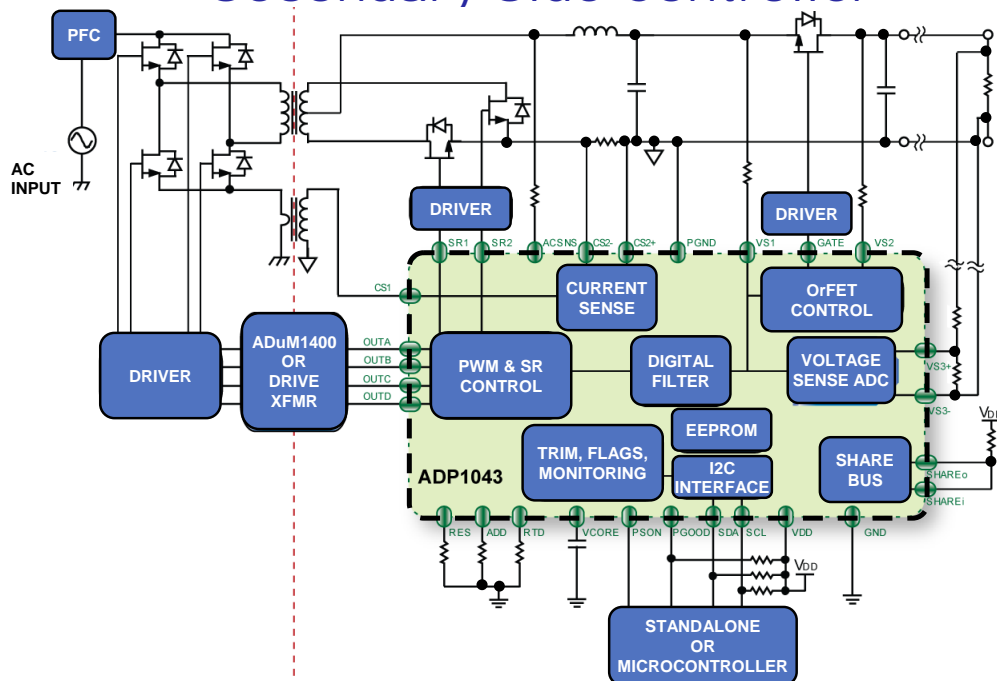
- ◆ **Integration of all typical controller functions**
  - Remote and local voltage sense
  - Both primary and secondary side current sense
  - PWM control
  - Synchronous Rectifier control
  - Digital or Analog Current Share Bus
- ◆ **Digital Control Loop**
  - Integrated filter
  - Filter can be adapted through software
    - ◆ Easier to maintain phase margin with voltage-mode controllers
    - ◆ Faster development time
    - ◆ Faster debugging
    - ◆ Option to compensate for temperature
  - Programmability through I<sup>2</sup>C
- ◆ **Digital control currently used in AC-to-DC primary-side converters and DC-to-DC secondary-side converters**

ADC technology in CMOS has progressed rapidly. The requirement for ADCs in digital power control is approximately 12 bits at sampling rates of a few MHz. This will obviously change due to product improvements, but represents the current requirement in primary and secondary-side power converters.

Other than increased reliability, functionality, power density, efficiency, reduced component count, etc., digital control offers design flexibility in the feedback control loop compensation. Current point-of-load supplies designed for powering high power microprocessors (such as Intel and AMD) are often manually adjusted on the system board for optimum load current step response. Digital adaptive feedback loop control and timing should eliminate this need.

Most analog switching converters use voltage-mode (VM), current-mode (CM), or a combination of the two in order to determine the value of feedback compensation values. Proper compensation of the feedback loop in order to maintain adequate phase margin in both the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is somewhat complicated. This is especially difficult when using only voltage-mode control. In a digital feedback control loop, the compensation is performed by digital filters whose characteristics can be easily changed depending on the mode of operation. This means that VM control is practical using adaptive digital filter techniques.

## Typical Application of ADP1043 Secondary-Side Controller



The ADP1043 is a secondary side digital power supply controller IC that is designed to provide all the functions that are typically needed in an isolated ac-to-dc or dc-to-dc control application. It is optimized for minimal component count, maximum flexibility, and minimum design time. Features include remote voltage sense, local voltage sense, primary and secondary side current sense, PWM control, synchronous rectifier control, and hot-swap sense and control. The control loop is digital, with an integrated programmable digital filter. Protection features include current limiting, ac sense, UVLO, and OVP (Overvoltage Protection).

The OrFET control feature allows multiple supplies to be connected in parallel.

The part supports current sharing and has an integrated programmable loop filter with an I<sup>2</sup>C interface. There is extensive on-chip fault detection and protection.

Fast calibration can be achieved using the on-chip 8 kB EEPROM, or and external microcontroller.

It should be noted that the ADM1041A secondary side controller uses traditional analog techniques.

## Programmability and Monitoring (Through I<sup>2</sup>C)

PROGRAMMABILITY	MONITORING
◆ Output Voltage Setting	◆ Output current
◆ Overcurrent (OCP) limit	◆ Output voltage
◆ Overvoltage (OVP) limit	◆ Output Line Impedance
◆ Undervoltage (UVP) limit	◆ Input current
◆ Overtemperature (OTP) limit	◆ Output power
◆ Soft-Start & Soft-Stop timing	◆ Duty cycle
◆ Loop filter poles and gains	◆ Current share bus
◆ PWM timing	◆ Temperature
◆ Duty cycle limits	
◆ OrFET On/Off trip voltage	

The use of the I<sup>2</sup>C bus provides both programmability and monitoring functions. This figure lists some of the various functions included by each.

# Powering Portable Systems

## Portable Power Considerations

- ◆ **Battery technology**
  - Lithium Ion battery of choice
  - NiMH and NiCd being phased out
- ◆ **Maximize battery life!**
  - Sleep and low power modes
  - Need efficient, small, low cost buck, boost, and buck-boost regulators as well as LDOs
- ◆ **Digital cameras, cell phones, PDAs, etc. require custom-tailored solutions**

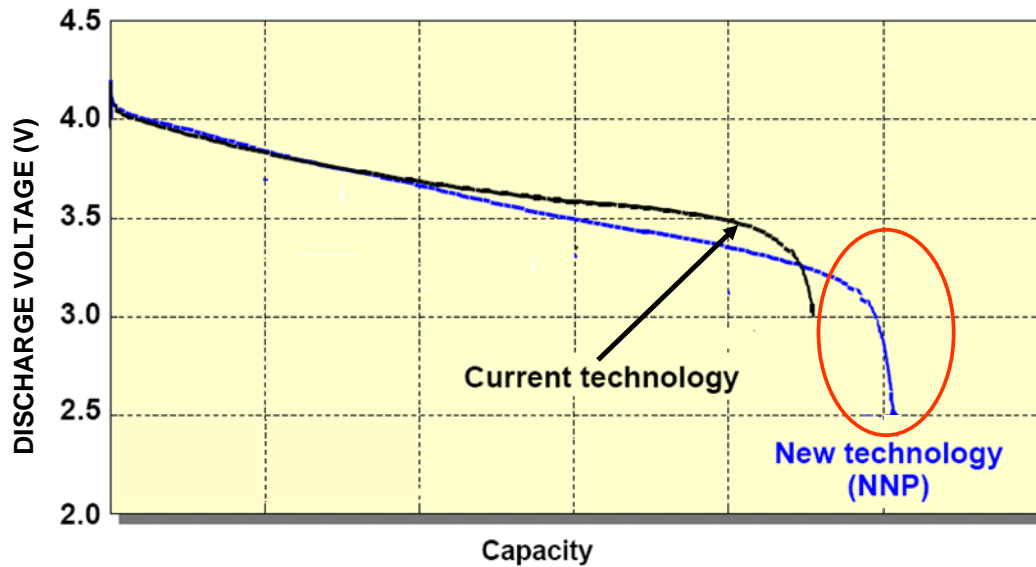


Modern portable systems depend highly on battery technology and efficient power management techniques. Maximizing battery life is a prime concern of portable equipment manufacturers.

Average power reduction techniques such as sleep, standby, or idle modes are required as well as efficient, small, low cost regulators.

Buck, boost, and buck-boost switching regulators as well as LDOs must be carefully integrated into the power chain of a portable system. In many cases, a custom-tailored power management IC is required for the specific application.

## The Energy System: Lithium Ion (Li-Ion)



NNP = Nickel-Based New Platform, Matsushita Battery Industrial Co., LTD

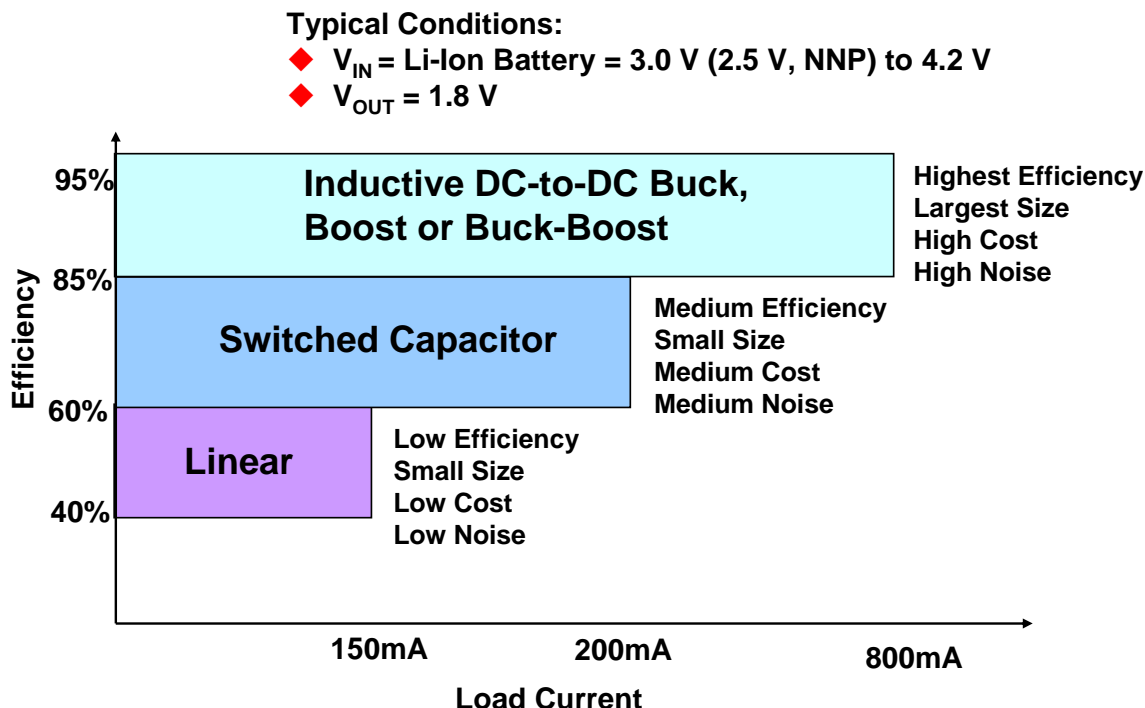
By far the most popular battery technology for today's portable systems is Lithium-Ion (Li-Ion). The discharge curve is shown here. New technology (NNP) extends the capacity of the battery and is available. "NNP" is an abbreviation for Nickel-Based New Platform Lithium-ion technology from Matsushita Battery Industrial Co., LTD. Work is on-going to produce even greater capacity in Li-Ion batteries.

The discharge curve shown here indicates that the usable battery voltage for current technology Li-Ion extends from 4.2V (fully charged) to 3.0 V (discharged). This means that the portable system power supply must provide the necessary output voltages over this fairly wide input voltage range. If the electronics require a 3.3 V supply, then it is clear that a buck-boost regulator is needed as the input voltage discharges from 4.2 V to 3.0 V.

The new Li-Ion technology discharges to 2.5 V, thereby lowering the usable battery voltage and increasing the probability of needing a buck-boost regulator.



## Techniques for Portable Power



There are three popular techniques for supplying portable power systems. The following guidelines apply specifically to a system powered by a single Li-Ion battery where the voltage ranges from 4.2 V to 3.0 V (2.5 V for NNP technology), and the output voltage is approximately 1.8 V.

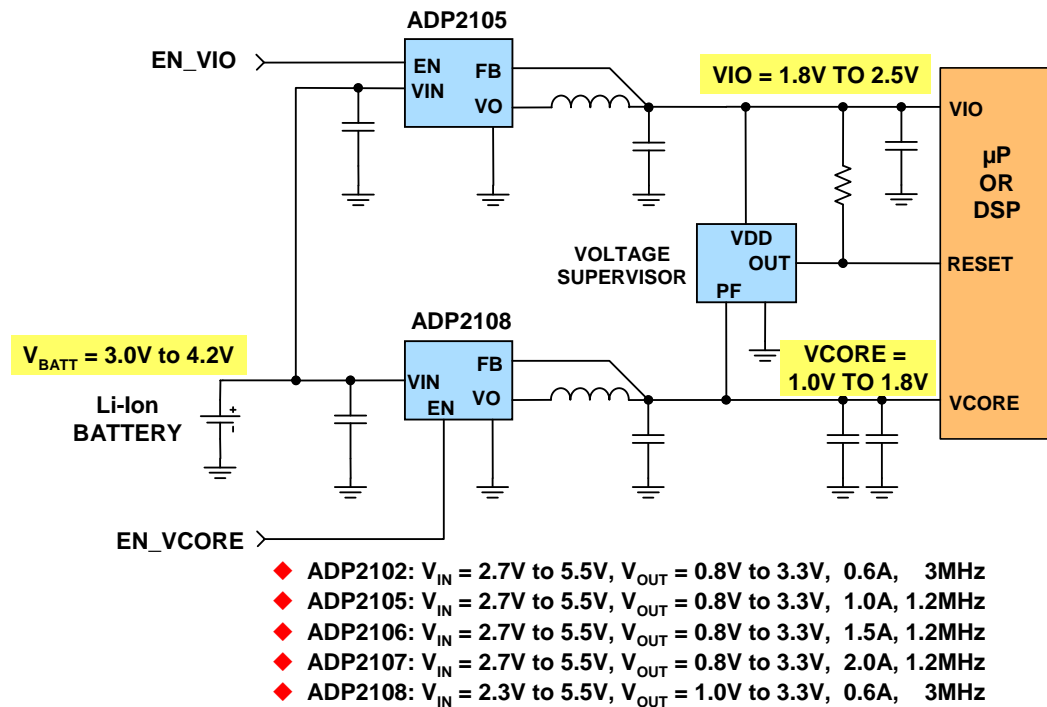
The inductive dc-to-dc buck, boost, or buck-boost regulator is the most efficient for higher currents, but takes up the most space and is generally the most costly of the three. Also the noise is the greatest.

The switched capacitor ("inductorless") regulator has medium efficiency, smaller size, lower cost, and less noise than the inductive regulators. However, the current capability is limited to approximately 200 mA.

The linear regulator (almost always an LDO) is by far the easiest to apply, the smallest, and has the lowest cost and noise of the three types. The efficiency of the LDO is approximately  $V_{OUT}/V_{IN}$ , so making general statements about their usage is somewhat dangerous. In applications where the  $V_{IN} - V_{OUT}$  voltage is low, the LDO may be an ideal choice if the current requirement is relatively low.

We will now look at a few typical applications in portable systems and see how efficient use can be made of the available power management building blocks.

## Processor Power Distribution with Separate Core and I/O Voltage

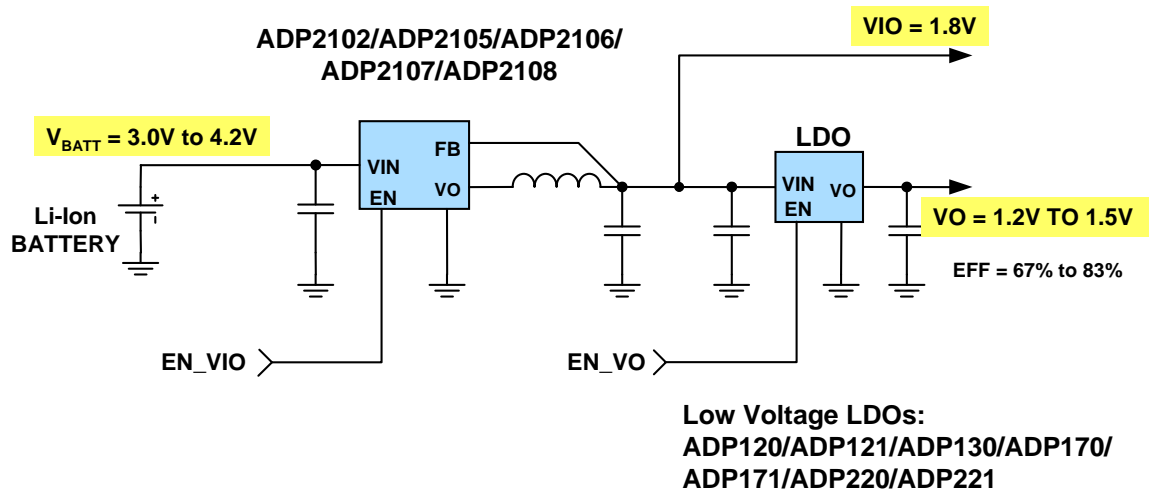


A common example in portable systems is generating the power for a microprocessor or DSP from a single Li-ion battery. As in "fixed" power applications, most modern microprocessors and DSPs for portable systems require a separate I/O and core voltage.

In this application, the ADP2105 synchronous buck regulator generates the I/O voltage which can be between 1.8 V and 2.5 V depending on the processor. The maximum current output is 1 A. The ADP2108 would also work if the current requirement is less than 600 mA.

The 1.0 V to 1.8 V core voltage is supplied by the ADP2108 synchronous buck regulator which can handle up to 600 mA.

## Typical Application Using a Switching Regulator and an LDO in Cascade



In the case where  $V_{IN} - V_{OUT}$  and the load current are both small, LDOs offer a simple, low cost, low noise regulator solution.

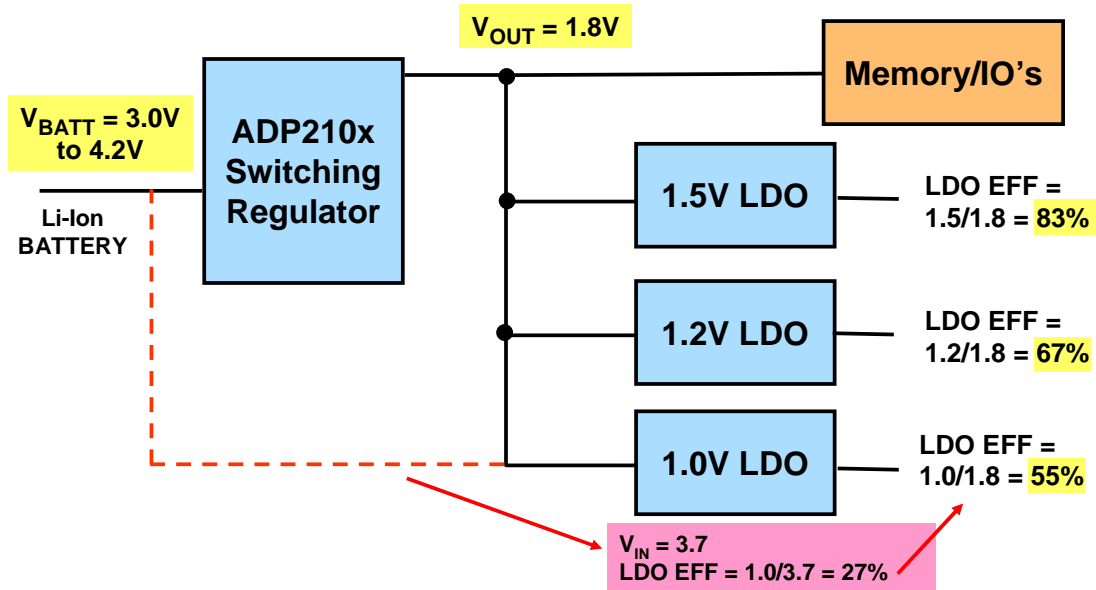
In this example, the LDO is in cascade with the 1.8 V switching regulator output. The LDO efficiency ( $V_{OUT}/V_{IN}$ ) ranges from 67% to 83% for output voltages between 1.2 V and 1.5 V.

## Point-of-Use Regulation Using LDOs with Low $V_{IN} - V_{OUT}$

Efficiency improves from

27-40% to 55-83% by Operating LDOs on 1.8V

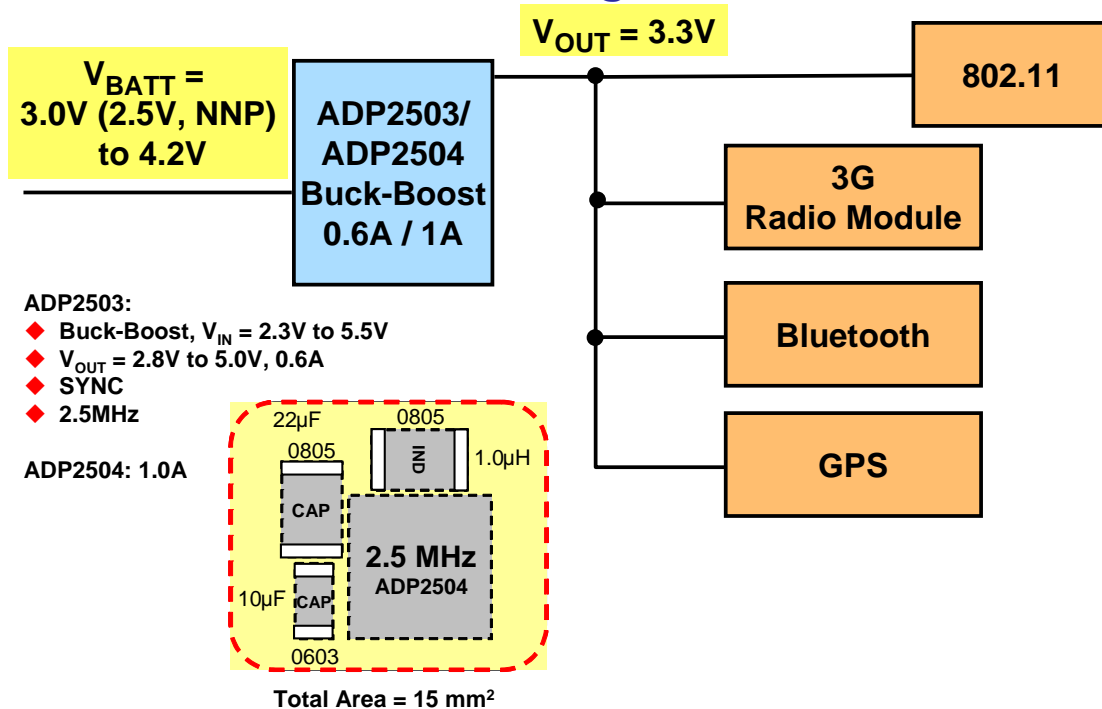
Low Voltage LDOs: ADP120/ADP121/ADP130/ADP170/ADP171/ADP220/ADP221



In this application, LDOs are driven from the ADP210x switching regulator 1.8 V output and provide efficiencies between 55% and 83% for output voltages between 1.0 V and 1.5 V.

Without the intermediate bus voltage of 1.8 V, the 1.0 V LDO efficiency drops to 27% if driven directly from the Li-Ion battery with a nominal voltage of 3.7 V.

## Buck-Boost Regulators Often Needed for Low Voltage Batteries

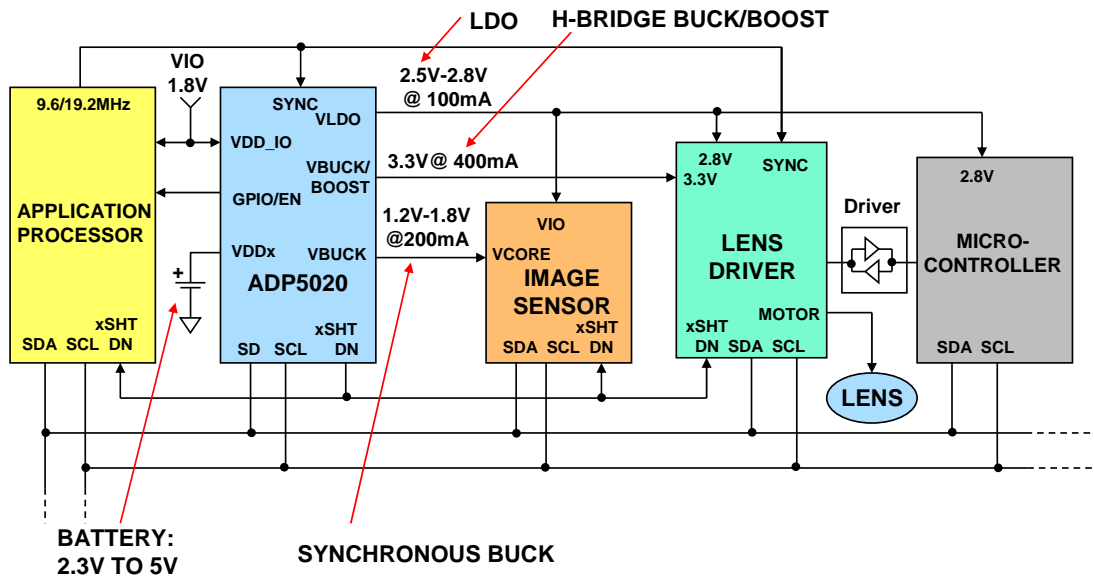


A common problem in portable systems is providing a switching regulator output when the input voltage from a discharging battery drops below the output voltage.

In this application, the switching regulator must supply a constant 3.3 V output as the input battery voltage discharges from 4.2 V to 2.5 V. This requires a switching regulator that can switch from the buck mode to the boost mode (buck-boost) while maintaining output regulation. The ADP2503 and ADP2504 are examples of buck-boost regulators that can supply 0.6 A and 1 A output currents, respectively, for input voltages from 2.3 V to 5.5 V.

Because of the high switching frequency of 2.5 MHz, small components can be used as shown to yield a solution that occupies only 15 mm<sup>2</sup> as shown in the figure, which uses a 1 μH ceramic inductor in an 0805 package.

## Integrated Camera Module Solution



This figure shows an integrated power solution for a camera module. The ADP5020 controller provides the following outputs:

1. 3.3 V, 400 mA buck-boost output based on an H-bridge FET controller.
2. 1.2 V to 1.8 V buck output capable of 200 mA for core voltage.
3. 2.5 V to 2.8 V 100 mA LDO output.

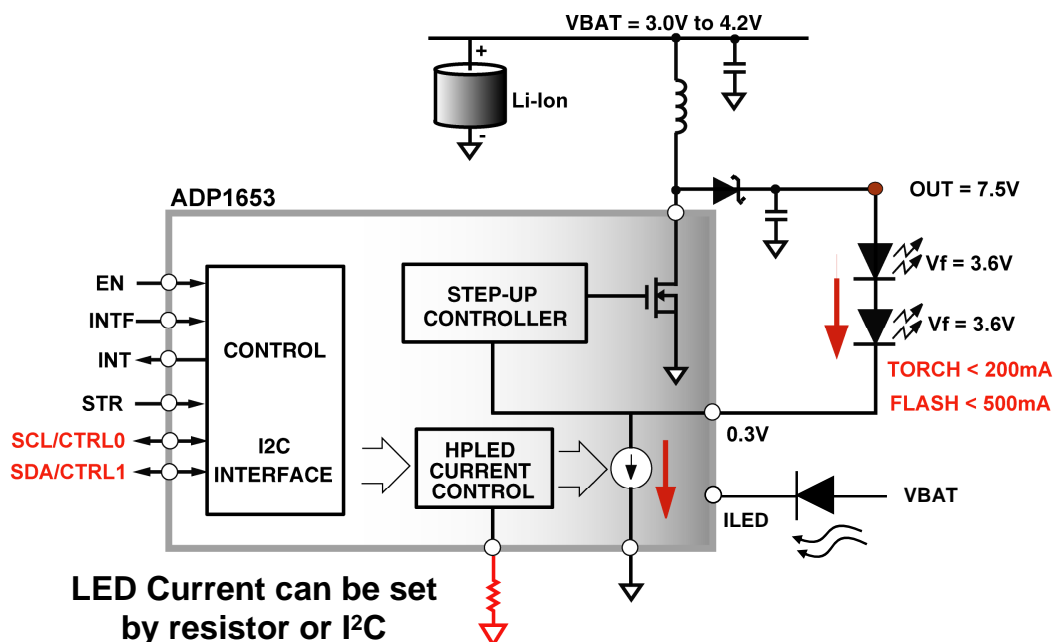
The device operates on an input voltage range of 2.3 V to 5.0 V, thereby covering all popular battery types.

The internal switching frequency of the regulators is 3 MHz.

The digital interface is I<sup>2</sup>C.

The figure shows the interface of the ADP5020 with the application process, image sensor, lens driver, and microcontroller.

## ADP1653 Flash LED Driver Requires Boost Regulator



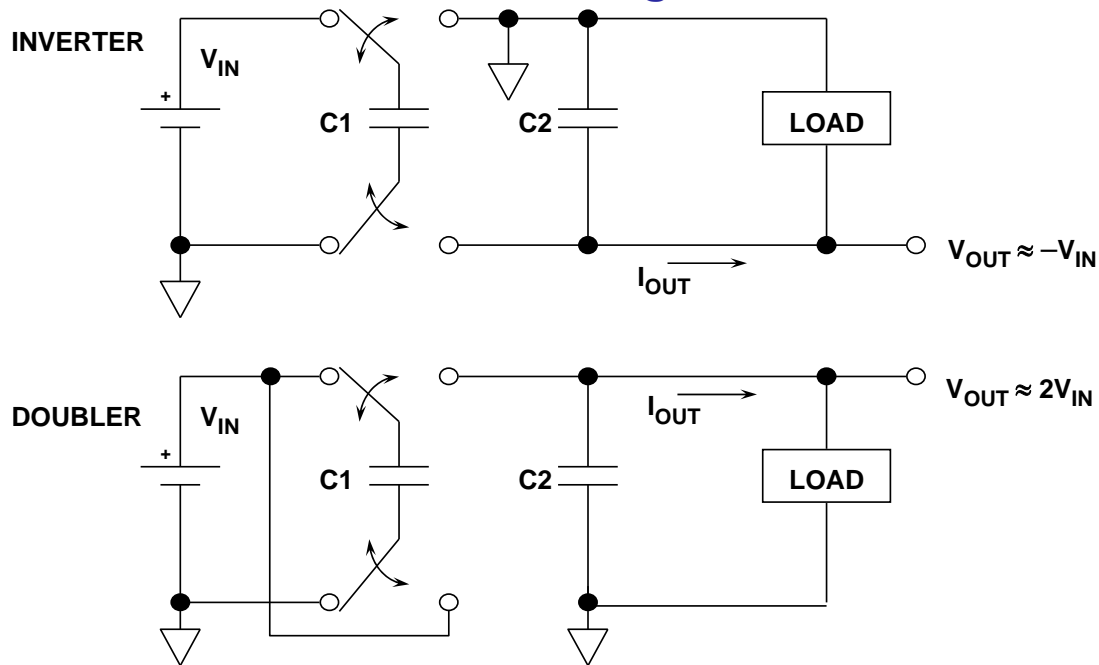
An excellent example of a boost regulator application is in a flash LED driver. The system typically operates on a single Li-ion battery (3.0 V to 4.2 V), but at least 7.5 V is required for the diode bias voltage. Flash systems generally use two LEDs in series, so the total voltage drop across the two diodes in the flash mode is  $3.6 \times 2 = 7.2$  V. The current source shown in the figure needs a headroom of 0.3 V, so the total diode bias voltage required is 7.5 V. This voltage is generated by the ADP1653 boost regulator. The LED current can be set by a resistor or programmed using the I<sup>2</sup>C interface.

The ADP1653 is a very compact, high efficiency, high power, camera-flash LED driver optimized for cellular phones. The device's high efficiency and dynamic LED current control improve flash brightness and picture quality in dimly lit environments. Efficiency peaks at 92% and is higher than charge pump solutions over the Li-ion battery range.

The device has a dual-mode interface that is configurable to 2-bit logic or an I<sup>2</sup>C interface. The indicator LED and high power LED currents are programmable with external resistors or through the I<sup>2</sup>C interface. To maximize overall flash brightness, the ADP1653 offers an input to reduce flash LED current in less than 50  $\mu$ s, referred to as the Tx mask. Tx masking reduces battery stress by scaling back flash LED current during an RF transmission.

The ADP1653 solution requires only four external components in I<sup>2</sup>C mode and fits in a 6.4 mm  $\times$  7.2 mm space. The part integrates multiple safety features such as soft start, flash timeout, output current limit, thermal protection, and overvoltage protection.

## Basic Switched Capacitor Voltage Inverter and Voltage Doubler



We have seen how inductors can be used to transfer energy and perform voltage conversions. This section examines switched capacitor voltage converters which accomplish energy transfer and voltage conversion using capacitors.

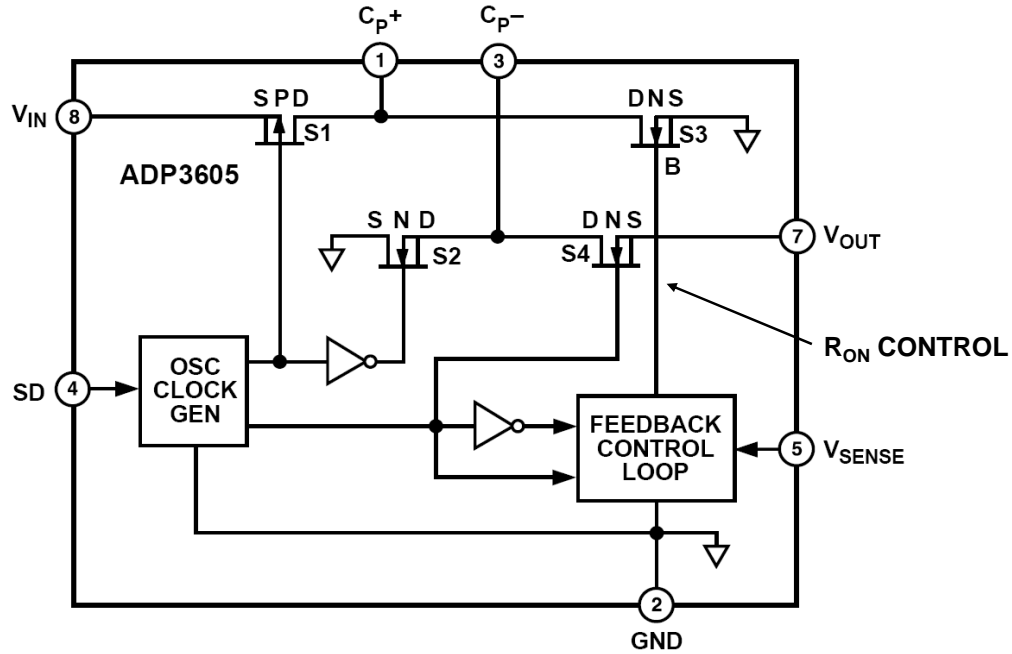
The two most common switched capacitor voltage converters are the voltage inverter and the voltage doubler circuit shown in the figure. In the voltage inverter, the charge pump capacitor,  $C1$ , is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle, its voltage is inverted and applied to capacitor  $C2$  and the load. The output voltage is the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle—defined as the ratio of charging time for  $C1$  to the entire switching cycle time—is usually 50%, because that generally yields the optimal charge transfer efficiency.

After initial start-up transient conditions and when a steady-state condition is reached, the charge pump capacitor only has to supply a small amount of charge to the output capacitor on each switching cycle. The amount of charge transferred depends upon the load current and the switching frequency. During the time the pump capacitor is charged by the input voltage, the output capacitor  $C2$  must supply the load current. The load current flowing out of  $C2$  causes a droop in the output voltage which corresponds to a component of output voltage ripple. Higher switching frequencies allow smaller capacitors for the same amount of droop. There are, however, practical limitations on the switching speeds and switching losses, and switching frequencies are generally limited to a few hundred kHz.

The voltage doubler works similarly to the inverter; however, the pump capacitor is placed in series with the input voltage during its discharge cycle, thereby accomplishing the voltage doubling function. In the voltage doubler, the average input current is approximately twice the average output current.

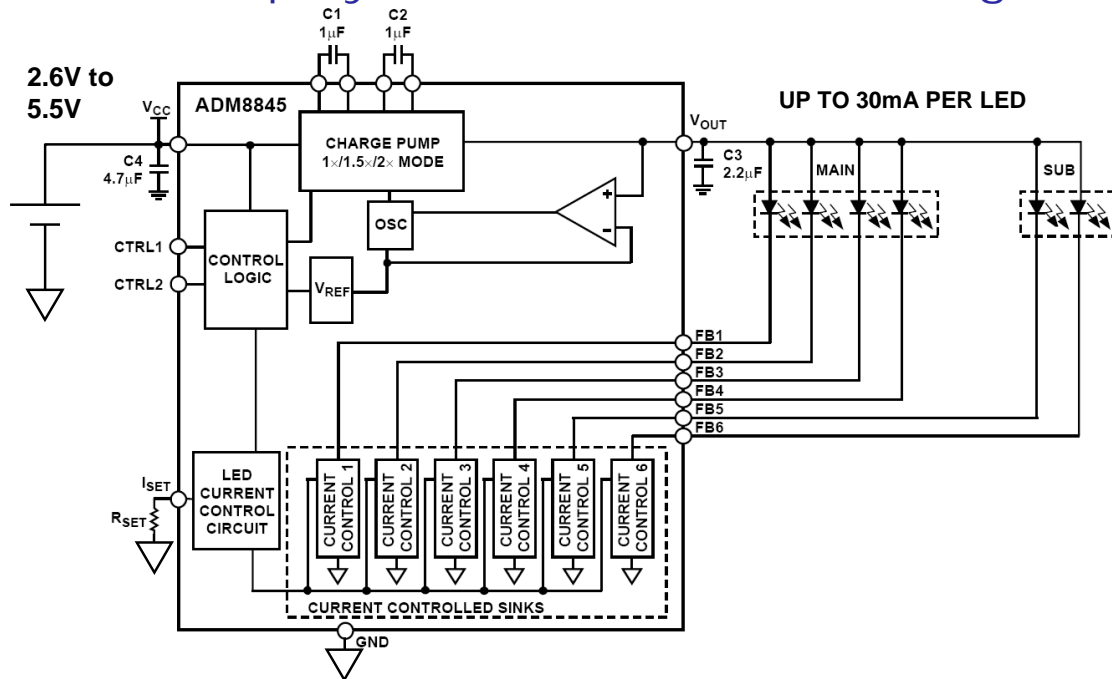


## ADP3605 120mA Switched Capacitor Inverter with Regulated Output



By far the simplest and most effective method for achieving regulation in a switched capacitor voltage converter is to use an error amplifier to control the on-resistance of one of the switches as shown in this figure, a block diagram of the ADP3605 120 mA voltage inverter. This device offers a regulated  $-3\text{ V}$  output for an input voltage of  $+3\text{ V}$  to  $+6\text{ V}$ . The output is sensed and fed back into the device via the  $V_{\text{SENSE}}$  pin. Output regulation is accomplished by varying the on-resistance of one of the MOSFET switches as shown by the control signal labeled " $R_{\text{ON}}$  CONTROL" in the diagram. This signal accomplishes the switching of the MOSFET as well as controlling the on-resistance.

## ADM8845 Charge Pump Driver for LCD Displays with White LED Backlights



The ADM8845 uses charge pump technology to provide the power required to drive up to six LEDs. The LEDs are used for backlighting a color LCD display, having regulated constant current for uniform brightness intensity. The main display can have up to four LEDs, and the sub display can have one or two LEDs. The digital CTRL1 and CTRL2 input control pins control the shutdown operation and the brightness of the main and sub displays.

To maximize power efficiency, the charge pump can operate in a 1×, 1.5×, or 2× mode. The charge pump automatically switches between 1×, 1.5×, and 2× modes, based on the input voltage, to maintain sufficient drive for the LED anodes at the highest power efficiency.

Improved brightness matching of the LEDs is achieved by a feedback pin to sense individual LED current with a maximum matching accuracy of 1%.

## Technical References

## Analog Devices' Technical References

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. See Chapter 9.
2. Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410. See Chapter 7.
3. Walt Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN: 0-916550-26-5. Also available as *Op Amp Applications Handbook*, Elsevier-Newnes, 2004, ISBN: 0-7506-7844-5. See Chapter 7.
4. Sridhar Gurram, Oliver Brennan, Tim Wilkerson, "DC-to-DC Switching-Regulator Insights—Achieving Longer Battery Life in DSP Systems," *Analog Dialogue* 41-12, December 2007.

## Practical Power Solutions

1. Point-of-Load Power
2. System Power Management and Portable Power
3. Power for Mixed Analog/Digital Systems
4. Hardware Design Techniques

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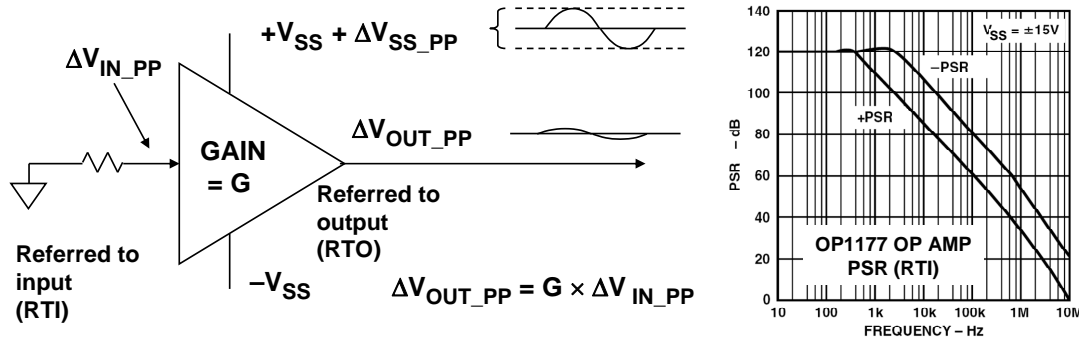
### SECTION 3

#### POWER FOR MIXED ANALOG/DIGITAL SYSTEMS

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# **General Guidelines for Powering Analog Circuits**

## Power Supply Rejection (PSR) vs. Frequency Is a Key Specification



- ◆  $PSRR = \frac{\Delta V_{SS\_PP}}{\Delta V_{OUT\_PP}}$  We will use this convention which gives a positive value for PSR in dB
- ◆  $PSR\ (dB) = 20 \log_{10} PSRR$
- ◆ PSRR and PSR are often used interchangeably, and the value in dB can be + or –
- ◆ Dual supply devices have separate specifications for + and – supplies,  $+PSR$ ,  $-PSR$
- ◆ PSRR and PSR are often used interchangeably,

The ability of an electronic device to reject power supply ripple and noise is key to determining the ripple and noise allowable on its power inputs. Ripple and noise rejection ability is specified as the PSRR (Power Supply Rejection Ratio). We will use an op amp as an initial example.

If the supply of an op amp changes, its output should not, but it typically does. If a change of X volts in the supply produces an output voltage change of Y volts, then the PSRR on that supply (referred to the output, RTO) is X/Y. The dimensionless ratio is generally called the power supply rejection ratio (PSRR), and Power Supply Rejection (PSR) if it is expressed in dB. However, PSRR and PSR are almost always used interchangeably.

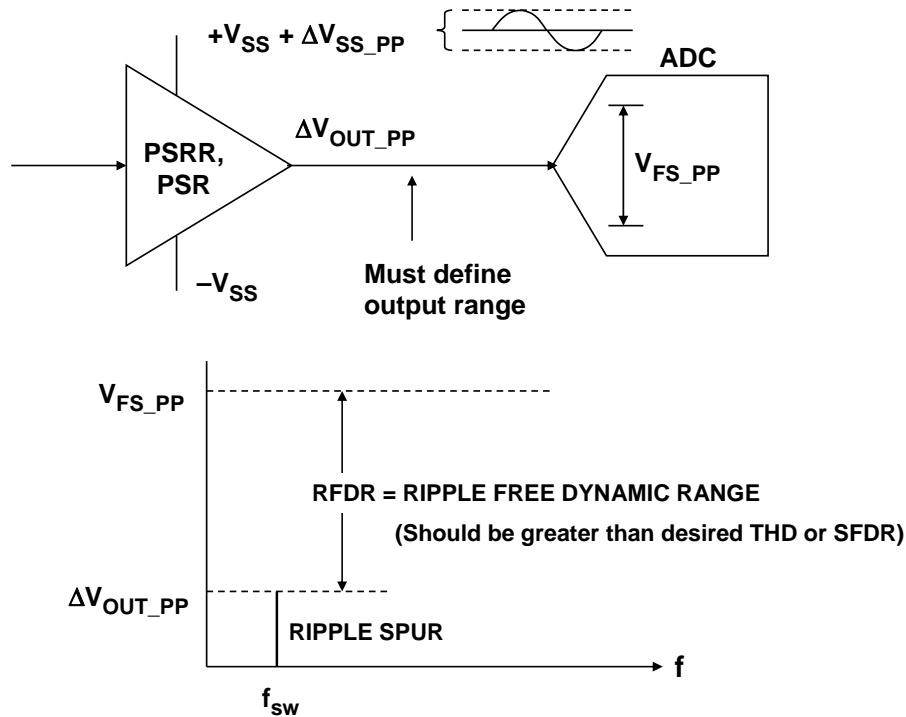
PSRR or PSR can be referred either to the output (RTO) or the input (RTI). The RTI value can be obtained by dividing the RTO value by the amplifier gain. In the case of the traditional op amp, this would be the noise gain. The data sheet should be read carefully, because PSR can be expressed either as an RTO or RTI value.

PSR can be expressed as a positive or negative value in dB, depending on whether the PSRR is defined as the power supply change divided by the output voltage change, or vice-versa. There is no accepted standard for this, and both conventions are in use.

If the amplifier has dual supplies, it is customary to express PSR separately for each.

It is extremely important to remember that PSR is very much a function of ripple or noise frequency as shown in the plot for the OP1177 op amp. In most cases, the roll-off follows that of the open-loop gain, and the slope is approximately 6 dB per octave (20 dB per decade).

## Definition of Ripple Free Dynamic Range



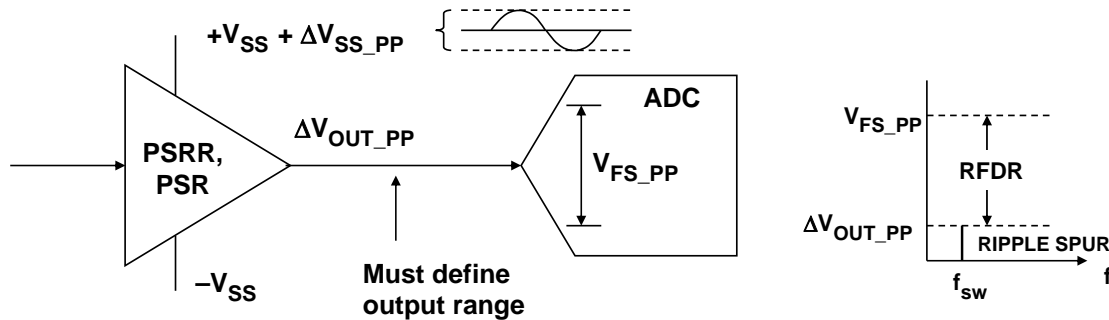
The amplifier output ripple voltage is not very useful unless it is compared to the dynamic range of the signal. If the amplifier drives an ADC, then the full-scale input voltage,  $V_{FS\_PP}$ , or the ADC defines the signal range. If the amplifier drives another amplifier, then the signal range is defined by the output range of the second amplifier divided by the gain of the second amplifier.

The Ripple Free Dynamic Range, RFDR, is defined as the ratio of the full-scale signal range to the output ripple spur, expressed in dB.

Many systems have requirements on harmonic distortion, or spurious free dynamic range (SFDR). It is therefore important that the ripple-free-dynamic-range be greater than the desired harmonic distortion or SFDR.



## Determine the Device's Sensitivity to Ripple by Calculating the RFDR at the Switching Frequency



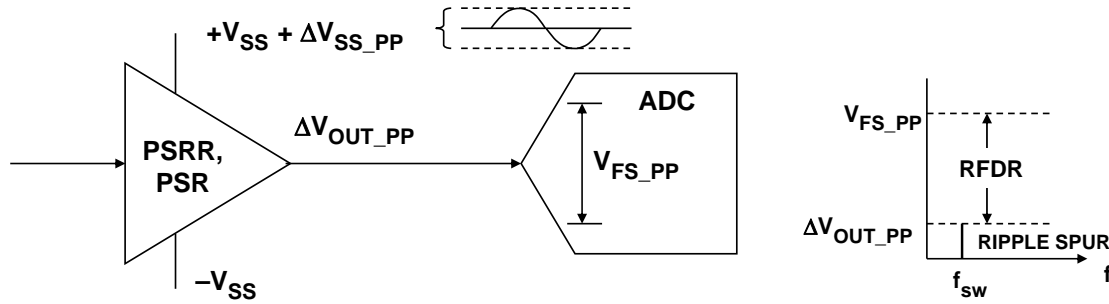
- ◆  $PSRR = \frac{\Delta V_{SS\_PP}}{\Delta V_{OUT\_PP}}$
- ◆  $PSR (dB) = 20 \log_{10} PSRR$
- ◆  $\Delta V_{OUT\_PP} = \Delta V_{SS\_PP} / PSRR$
- ◆ "RIPPLE FREE" DYNAMIC RANGE (RFDR) =  $20 \log \frac{V_{FS\_PP}}{\Delta V_{OUT\_PP}}$
- ◆  $RFDR = PSR + 20 \log \frac{V_{FS\_PP}}{\Delta V_{SS\_PP}}$

The PSR specification can be used to calculate the amplifier output ripple, and the output ripple amplitude can then be compared to the signal range. The signal range must be specified in order for the calculated output ripple to be meaningful.

In most cases, an ADC will determine the signal range. In some cases it is determined by the compression point of an amplifier further downstream in the signal path.

Once the dynamic range is defined, the ripple-free-dynamic-range is easily calculated as shown in the figure.

## Example Calculation of Maximum Allowable Power Supply Ripple Voltage



$$\diamond \quad \Delta V_{SS\_PP} \leq V_{FS\_PP} \times 10^{-\left[\frac{RFDR - PSR}{20}\right]}$$

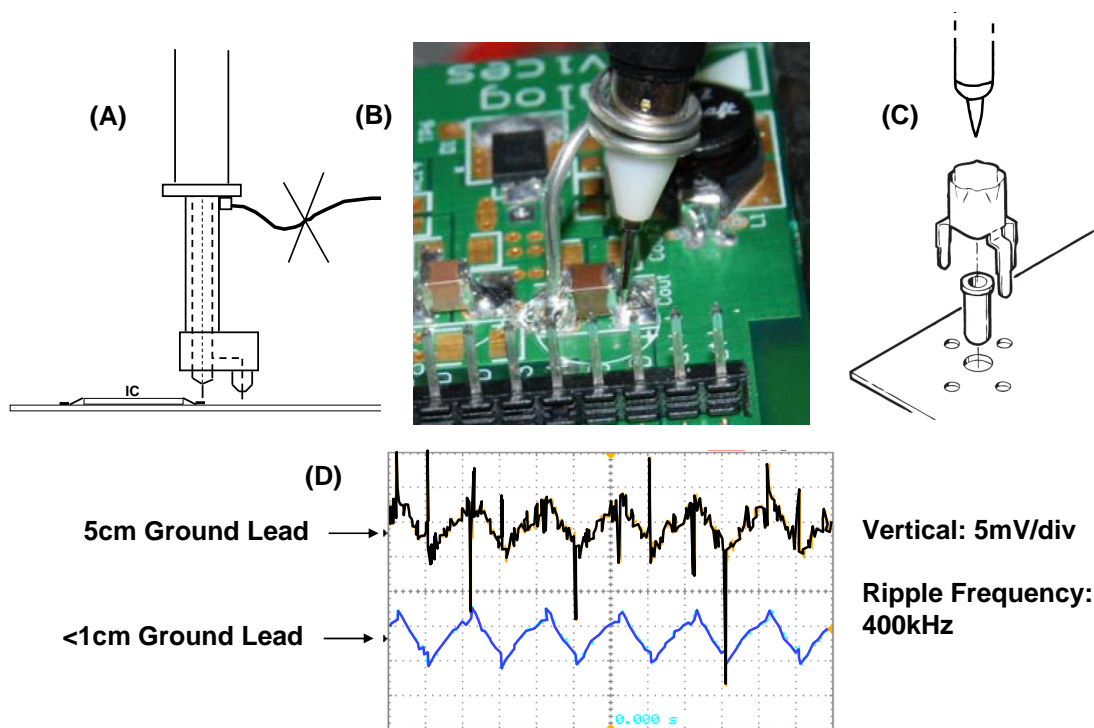
**Example:**  $V_{FS\_PP} = 2.0V$ ,  $RFDR = 100dB$ ,  $PSR = 60dB$

Then  $\Delta V_{SS\_PP} \leq 20mV$

The equation for RFDR in the previous figure can be rearranged and solved for the maximum allowable power supply ripple,  $\Delta V_{SS\_PP}$ , for a required RFDR and a given PSR.

The example shows that for a full-scale range of  $V_{FS\_PP} = 2V$ , a ripple free dynamic range of 100 dB, and a PSR of 60 dB, the peak-to-peak power supply ripple must be less than 20 mV.

## Measuring Ripple



Simply obtaining an accurate measurement of power supply ripple can be a difficult task, especially due to switching noise.

Power supply ripple must be measured directly at the IC power pin. This can be difficult to do with an oscilloscope, because a standard probe ground clip lead of a few cm creates an effective antenna which picks up magnetic switching noise from the power supply as well as noise from other sources and translates it into voltage spikes as shown in (D).

The "bayonet" clip used in (A) reduces the ground probe length to less than 1 cm. A wire loop soldered to ground as in (B) is also an effective way to maintain a short connection to the ground plane.

The ideal method is to use a special probe tip adapter which solders directly to the PC board as shown in (C), but this technique is generally reserved for prototypes or test boards where frequent measurements are required.

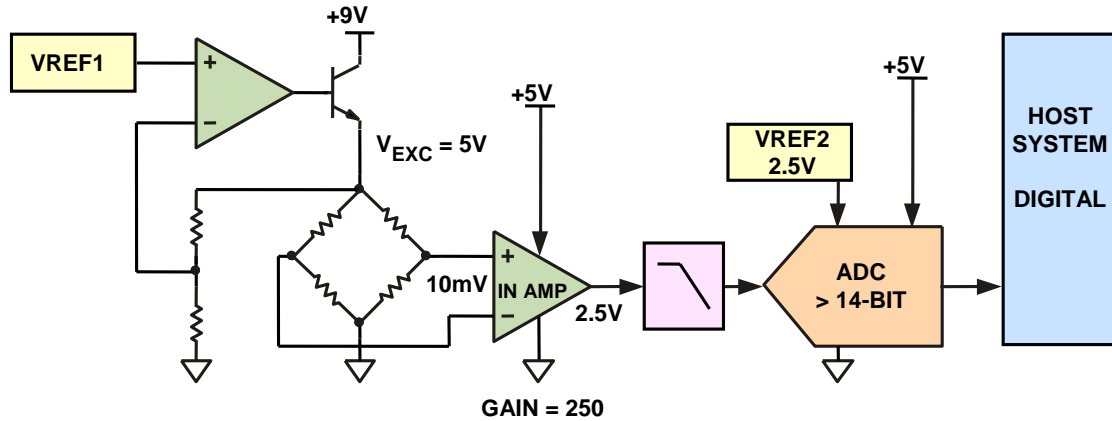
The scope trace capture in (D) shows the effect of reducing the ground lead from 5 cm to less than 1 cm. Note the dramatic reduction in the 400 kHz "spikes" which ride on the ripple voltage.

## Powering Amplifiers

[www.analog.com/amplifiers](http://www.analog.com/amplifiers)

In this section, we examine the PSR of various amplifiers to determine their sensitivity to power supply ripple.

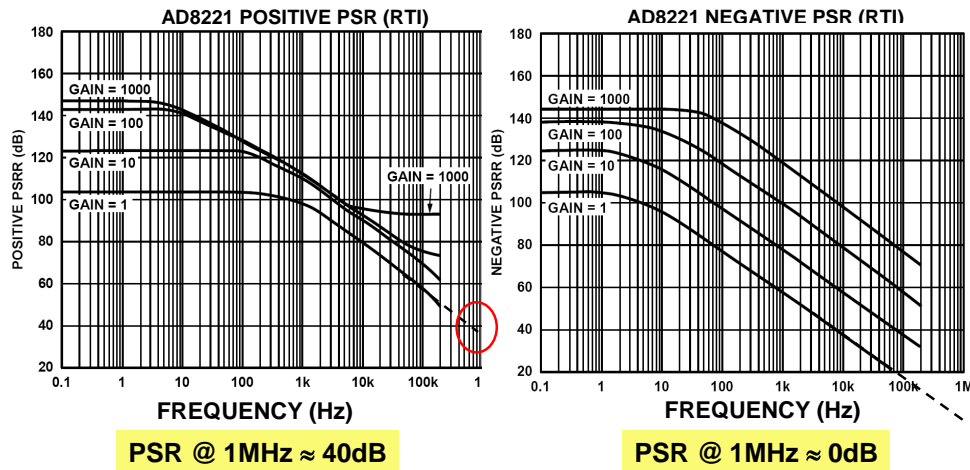
## **Typical Weigh Scale Application of Instrumentation Amplifier**



The instrumentation amplifier (in-amp) is a fundamental building block in practically all industrial measurement systems. This shows a typical application in a weigh scale signal processor.

The in-amp is set for a gain of 250 to amplify the full-scale load cell bridge output of 10 mV to "fill" the 2.5 V input range of the ADC.

## PSR for Representative In-Amps



### OTHER POPULAR IN-AMPS:

**AD623 SINGLE SUPPLY PSR @ 1MHz  $\approx$  0dB, G = 1**

**AD627 SINGLE SUPPLY PSR @ 1MHz  $\approx$  0dB, G = 5**

This shows the PSR of the industry-standard AD8221 in-amp as well as two newer single-supply devices. Note that the graph shows the PSR reflected to the input (RTI).

The PSR for the positive supply at 1 MHz is extrapolated to be approximately 40 dB, and the PSR of the negative supply is approximately 0 dB.

This poor PSR performance of in-amps is typical, and must be dealt with in all application circuits which use them. The following pages will discuss this critical issue in more detail.

## Instrumentation Amplifier Characteristics

- ◆ Instrumentation amplifiers are optimized for CMR and PSR at AC power line frequencies of 50Hz and 60Hz
- ◆ Gain, CMR, PSR falls off at 6dB/Octave above 100Hz
- ◆ Must assume 0dB PSR at switching frequencies above 500kHz
- ◆ Out-of-band signals on power or input will be rectified by internal junctions and create unwanted DC offsets (RFI Rectification)
- ◆ Must have excellent localized decoupling to filter noise and ripple frequencies if power supply is not clean

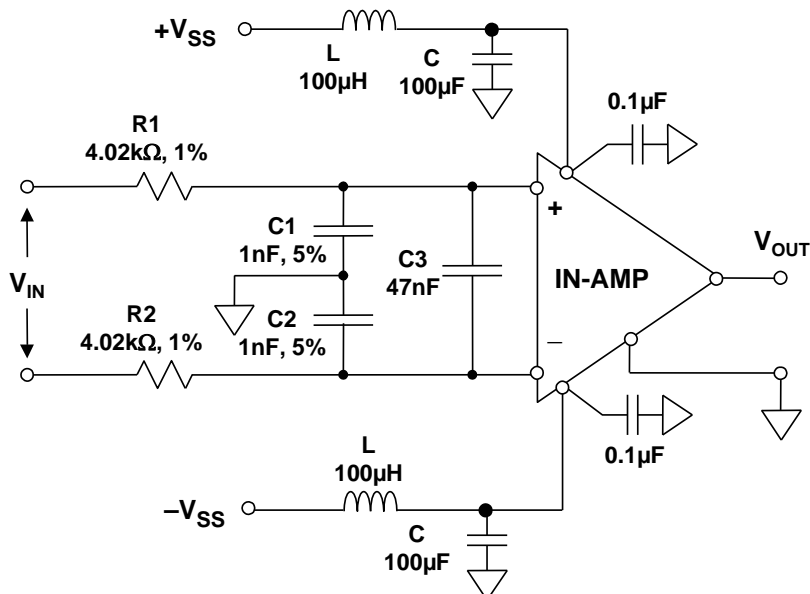
The in-amp is optimized for common-mode rejection (CMR) and PSR at ac power line frequencies of 50 Hz and 60 Hz.

The gain, CMR, and PSR generally drop off at 6 dB/octave above about 100 Hz.

High frequency ripple or noise outside this bandwidth which appears on the power supply or the input is rectified by internal junctions and creates unwanted dc offsets at the output. This process is called "RFI rectification."

For this reason, excellent localized decoupling must be applied to the in-amp power supply pins. The in-amp inputs usually require additional common-mode input filtering to prevent RFI rectification.

## In-Amp Input and Power Supply Filtering



$$\text{DIFFERENTIAL FILTER BANDWIDTH} = \frac{1}{2\pi (R1 + R2) \left[ \frac{C1 \cdot C2}{C1 + C2} + C3 \right]} = 417\text{Hz}$$

This shows a typical filtering network for the power supply and signal input of an in-amp. Let's look at the power supply networks first.

The input LC filter is designed to remove the ripple component of the power supply noise. The 100 µF electrolytic capacitors should be located within a couple of inches of the in-amp power pins. The ESR of the capacitors should be low, depending on the amount of ripple attenuation required. There is a detailed discussion later in this section regarding the design of the LC network.

The 0.1 µF ceramic capacitors are for high frequency decoupling. They should be located as close to the actual power pins as is physically possible, and the connection to the power pin and the ground plane should be as short as possible.

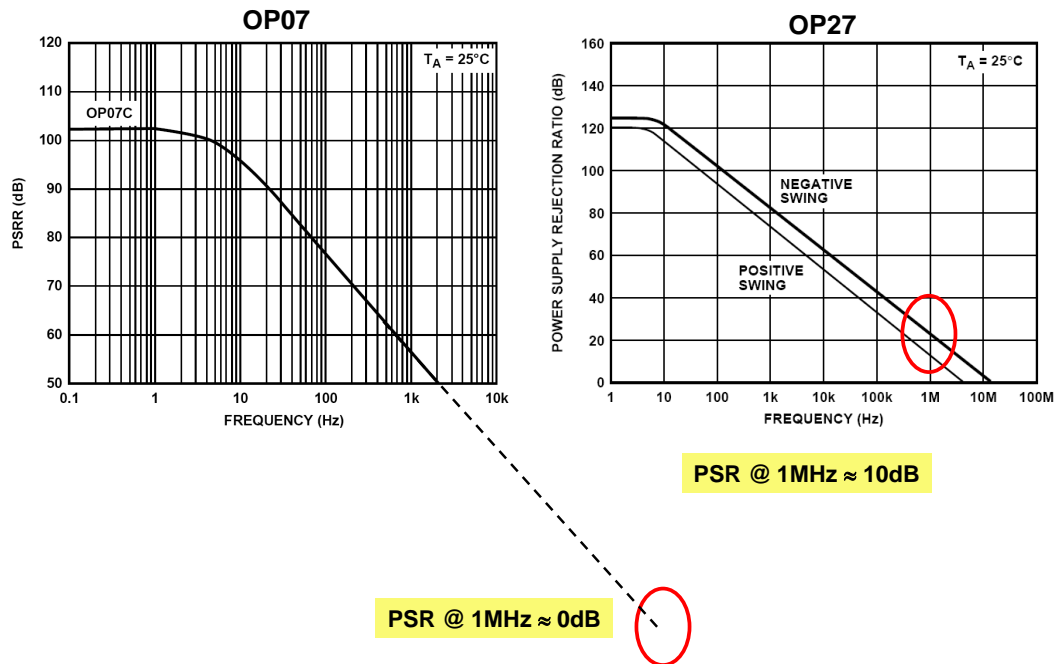
The input filter network is designed to reduce RFI rectification by rejecting common-mode signals outside the signal bandwidth.

The R1/C1 and R2/C2 networks filter the common-mode noise. The time constants should be well matched to prevent common-mode-to-differential mode conversion. For this reason, the resistors (R1, R2) should be 1%, and the capacitors (C1, C2) 5% or better. With the values shown, the common-mode filter bandwidth due to R1/C1 is approximately 40 kHz.

Because of the potential slight mismatch between the two time constants, C3 is added as a differential-mode filter. The resulting differential filter bandwidth is approximately 417 Hz.



## Industry-Standard OP07 and OP27 Precision Bipolar Op Amps PSR (RTI)

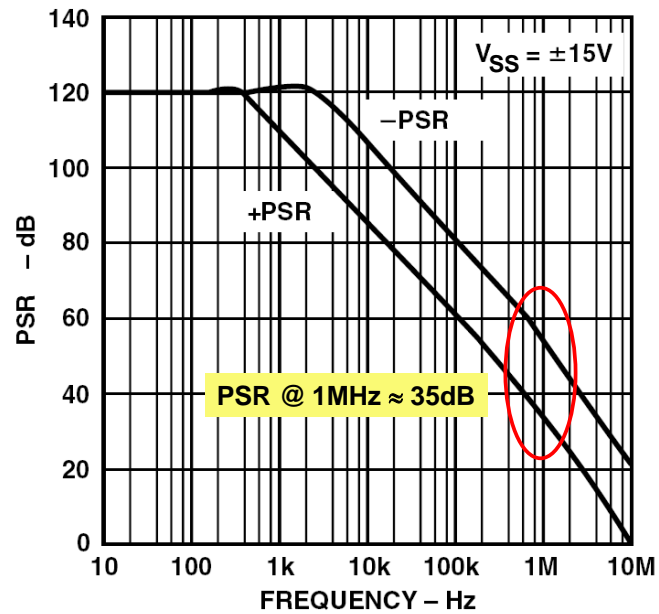


We now look at a couple of industry-standard precision bipolar op amps, the OP07 and the OP27. The OP07, designed by George Erdi and first introduced by PMI in 1975, became the "741" of precision op amps. It is still widely second-sourced today. The OP07 uses a trim technique called "zener zapping" to obtain offset voltages as low as  $25\ \mu\text{V}$  and drift rates of  $0.6\ \mu\text{V}/^\circ\text{C}$ . The unity gain bandwidth product of the OP07 is about 0.6 MHz.

Both the OP07 and OP27 use input bias current cancellation to achieve a low input bias current of less than  $\pm 10\ \text{nA}$ .

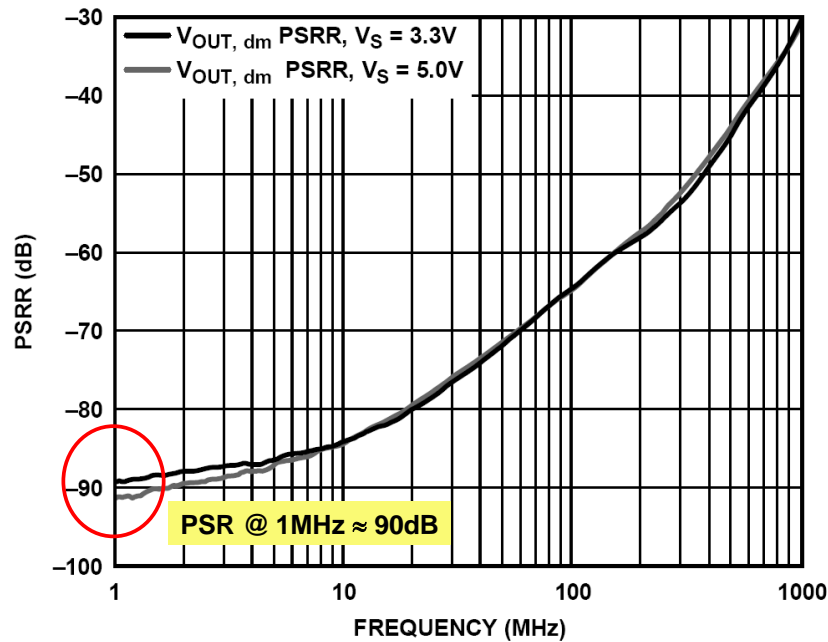
However, from a PSR standpoint these parts fall in about the same category as the in-amps previously discussed.

## **OP1177 Modern Precision Bipolar Op Amp PSR (RTI)**



The OP1177 is a modern version of a precision bipolar op amp and has a unity gain-bandwidth product of 1.3 MHz. It has approximately 25 dB better PSR than the OP07 or OP27.

## ADA4937-1, 1.9GHz, Low Distortion, 16-Bit, SiGe Differential ADC Driver (RTO)

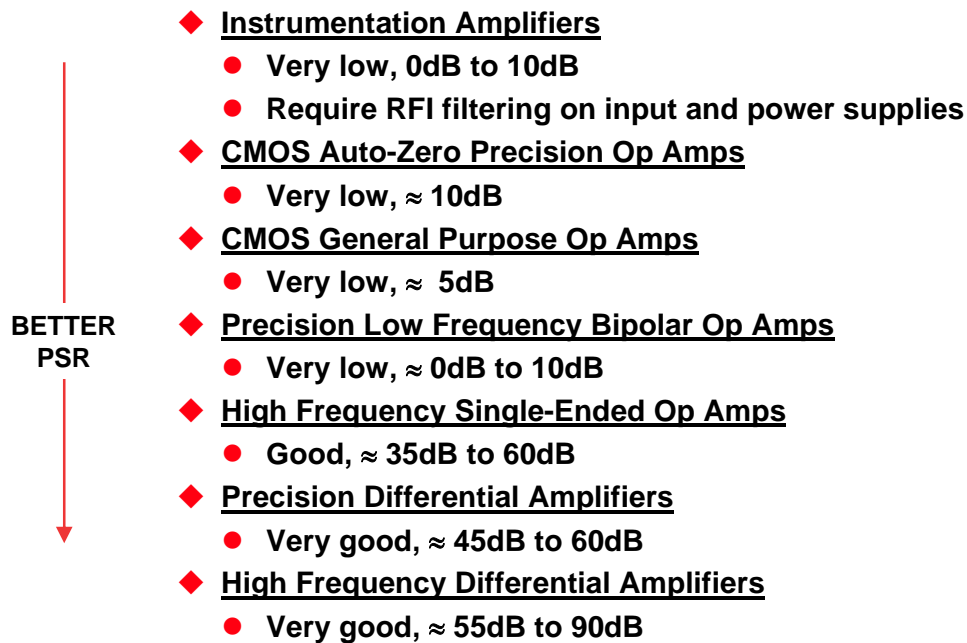


The trend in most high performance ADCs is to use differential inputs and differential techniques throughout the circuit as well as the digital outputs.

The differential input drivers for these converters have both high bandwidth and relatively good PSR as shown here for the ADA4937-1 differential driver.

The differential wideband nature of these parts gives them excellent CMR at high frequencies which helps the PSR.

## Amplifier PSR Summary



This summarizes the PSR of typical amplifiers.

Within a particular family, amplifiers with higher loop gain and bandwidth generally have better PSR.

In most cases, the higher speed amplifiers typically have better PSR, and the differential amplifiers have the highest.

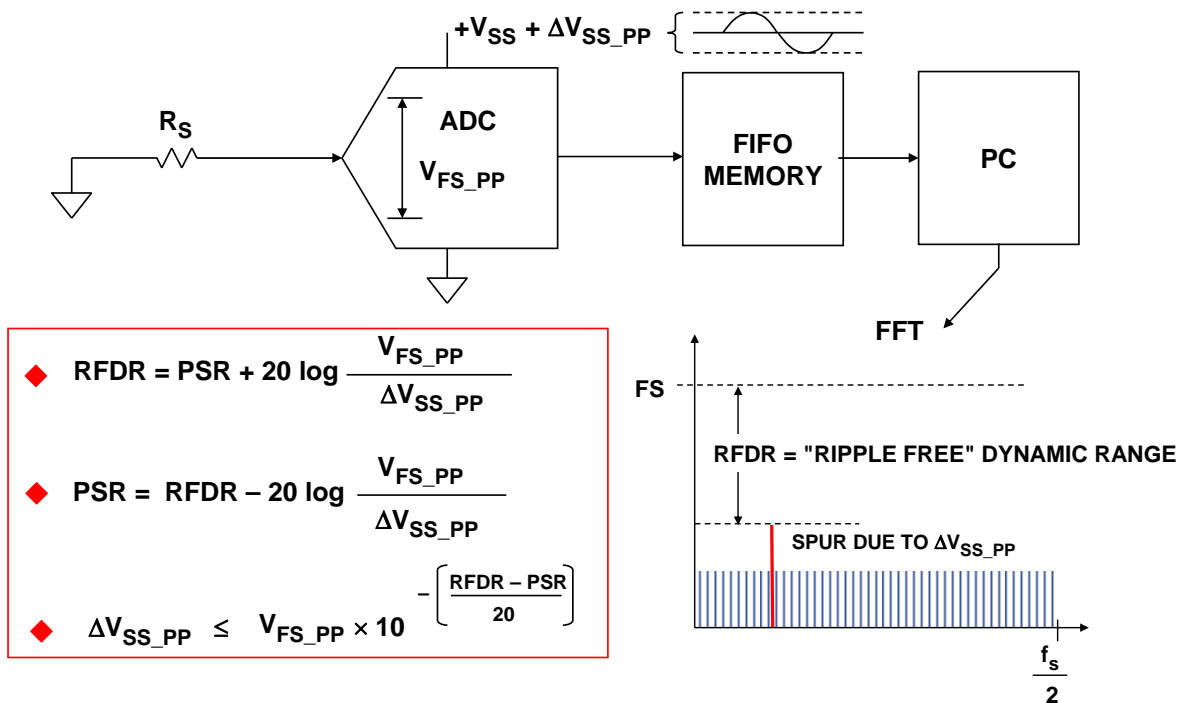
The bottom line is that while there seem to be some general trends, you must always consult the individual amplifier data sheet for specific PSR numbers.

The PSR at the maximum power supply switching frequency is a good measure of the sensitivity of amplifiers to ripple and noise.

## Powering ADCs

[www.analog.com/adcs](http://www.analog.com/adcs)

## Defining the PSR of an ADC in Terms of its Spectral Output



Defining the PSR for an ADC is somewhat more difficult than for an op amp. Because most ADCs are used in signal processing applications, the effects of power supply ripple on the output frequency spectrum are more important than the effects on static parameters such as offset or gain.

This figure shows a standard method for measuring the PSR of an ADC. The input to the ADC is grounded through a resistor, and the ripple free dynamic range (RFDR) is measured using standard FFT techniques. In the figure, the spur of interest is the spur that occurs at the power supply switching frequency.

The next step is to measure the peak-to-peak ripple on the ADC power supply pin,  $\Delta V_{SS\_PP}$ . The PSR is then calculated by the equation:

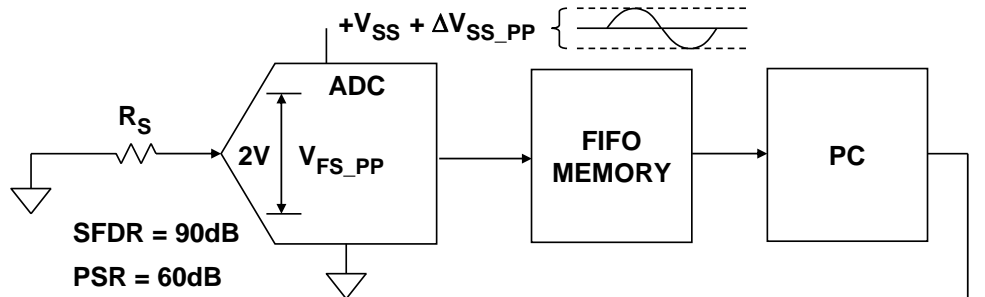
$$PSR = RFDR - 20 \log \frac{V_{FS\_PP}}{\Delta V_{SS\_PP}}$$

The second term in the equation normalizes the PSR with respect to the ADC full-scale input range.

If the ADC PSR specification and the RFDR requirement are known, the equation can be re-arranged to solve for the maximum allowable peak-to-peak ripple voltage:

$$\Delta V_{SS\_PP} \leq V_{FS\_PP} \times 10^{-\left(\frac{RFDR - PSR}{20}\right)}$$

## Example Calculation of Maximum Allowable Power Supply Ripple

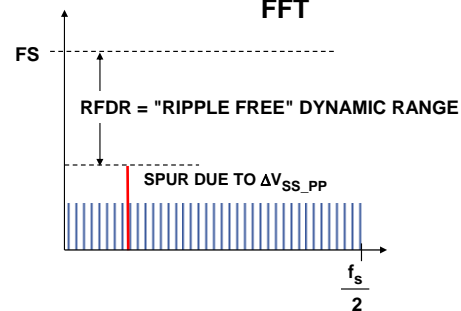


- ◆ The ADC Spurious Free Dynamic Range (SFDR) is 90dB
- ◆ The Ripple Free Dynamic Range (RFDR) should be at least 100dB
- ◆ The ADC PSR @ switching frequency is 60dB
- ◆ The ADC full scale voltage is  $V_{FS\_PP} = 2V$

$$\Delta V_{SS\_PP} \leq V_{FS\_PP} \times 10^{-\left[\frac{RFDR - PSR}{20}\right]}$$

- ◆ Substitute in above equation, solve for  $\Delta V_{SS\_PP}$

$$\Delta V_{SS\_PP} \leq 20mV$$



This example shows how the maximum allowable power supply ripple is determined based on the ADC specifications and desired frequency-domain performance.

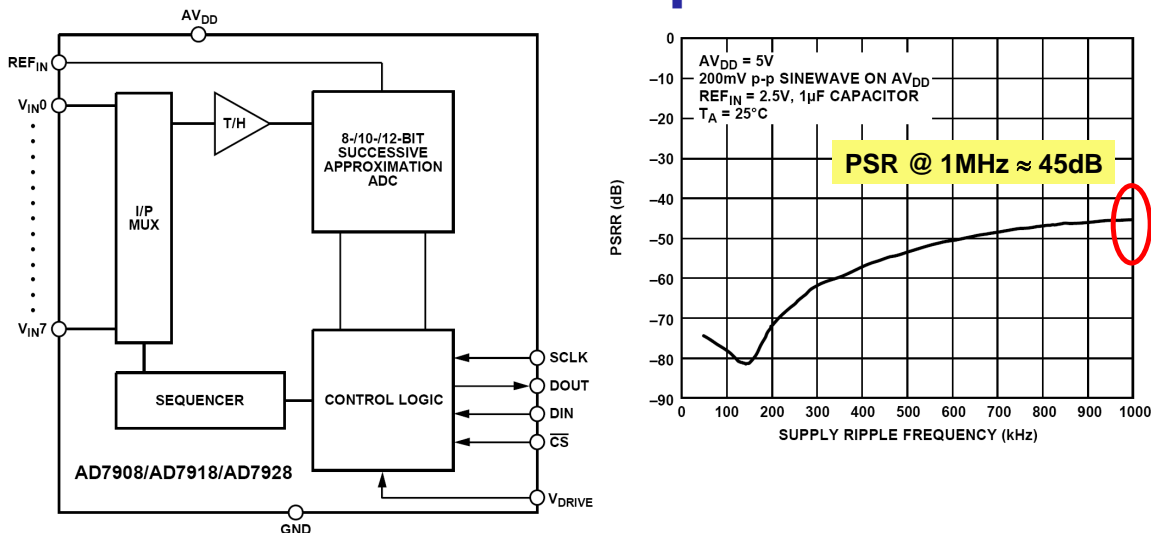
This ADC has an SFDR of 90 dB. The RFDR should be greater than this by at least 10 dB, so the RFDR requirement is 100 dB.

The PSR at the switching frequency is obtained from the ADC data sheet and is 60 dB (at the switching frequency).

The full-scale input range of the ADC is 2 V peak-to-peak.

The equation is solved for the maximum allowable ripple voltage, which in this case is 20 mV.

## Multichannel Data Acquisition System on a Chip



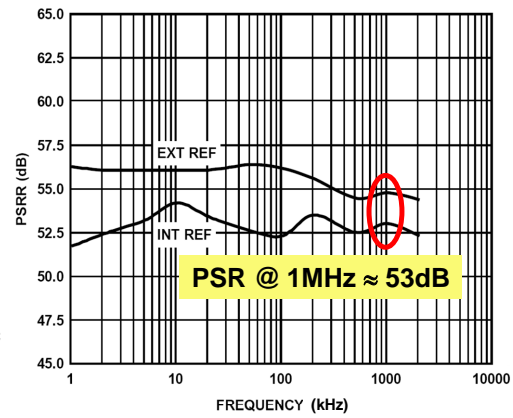
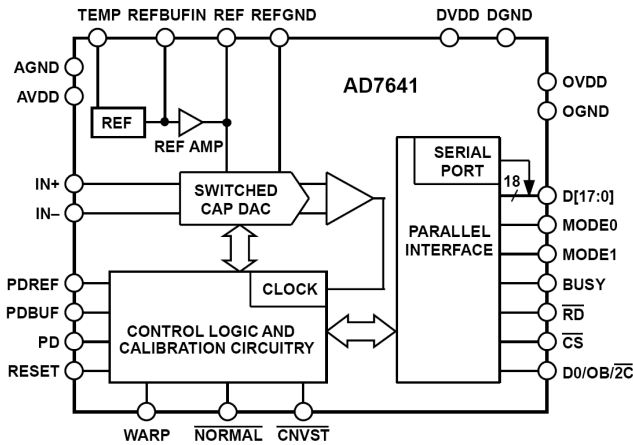
Now let's look at the PSR of several popular families of ADCs. There is little consistency between manufacturers regarding this specification, but the numbers presented here will give an idea of what to expect in an actual design.

This shows the PSR of a complete data acquisition system on a chip, the AD7908 (8-bit), AD7918 (10-bit), and AD7928 (12-bit) family. The architecture is typical of such systems and consists of an 8-channel input multiplexer, sample-and-hold, and a successive approximation (SAR) ADC.

The PSR of the device at 1 MHz is approximately 45 dB. This assumes an external 2.5 V reference with a 1  $\mu F$  decoupling capacitor on the  $REF_{IN}$  pin.



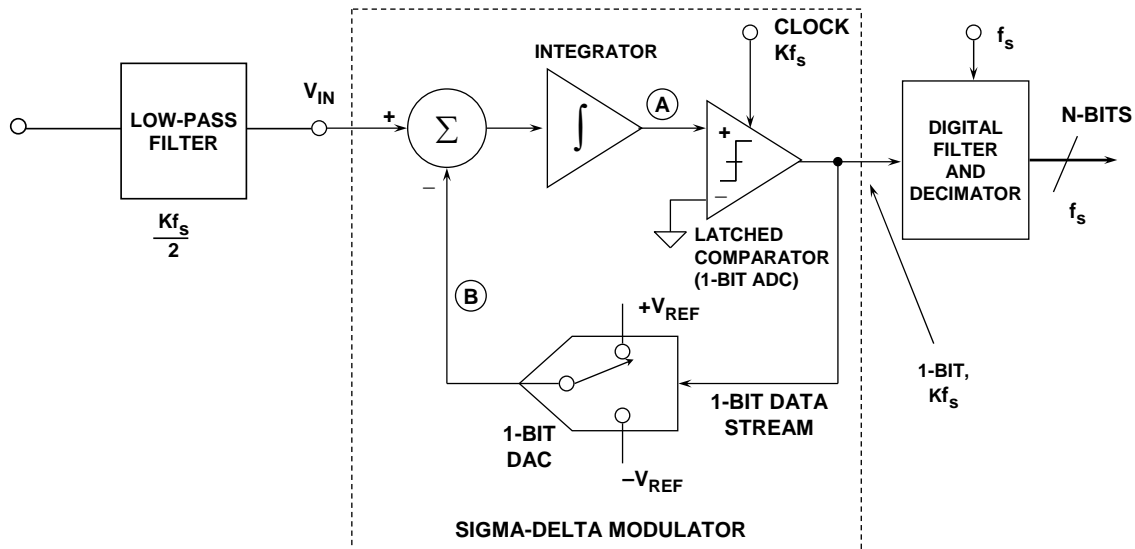
## AD7641 18-Bit, 2 MSPS, PuISAR® ADC



The PuISAR family of high performance successive approximation (SAR) ADCs all use differential techniques throughout the design, so the PSR is maintained across a fairly wide range of ripple frequencies.

This shows the AD7641 18-bit, 2 MSPS ADC PSR as approximately 53 dB at 1 MHz using the internal reference. Slightly better PSR can be obtained using an external reference.

## Integrator and Digital Filter Reduce the Effects of Power Supply Ripple in $\Sigma$ - $\Delta$ ADCs



Sigma-delta ADCs use a combination of oversampling, quantization noise shaping, and digital filtering in order to achieve up to 24 bits of resolution at sampling rates of up to 1 kSPS. These high resolution ADCs have virtually replaced the dual-slope type.

This is a block diagram of a sigma-delta ADC which shows the key functional blocks. The averaging nature of the sigma-delta modulator and the digital filter make this type of converter relatively insensitive to power supply ripple. DC power supply rejection as well as 50 Hz or 60 Hz rejection is typically 70 dB to 90 dB, but data sheets rarely specify the ac PSR for these devices.

## Sigma-Delta Power Considerations

- ◆ Typical throughput rates are less than a few kSPS for high resolutions (18+ bits)
- ◆ DC PSR is typically 70dB to 90dB
- ◆ AC PSR is not usually specified except at 50Hz and 60Hz power line frequencies
- ◆ Internal digital filter removes most ripple frequency components.
- ◆ Don't depend on the averaging effect of the digital filter to remove all the ripple components. Aliasing can still occur and put the ripple frequency into the signal bandwidth
- ◆ Broadband and ripple noise should be minimized with good localized decoupling of power pins at the IC, especially important for 20+ bit devices
- ◆ Consider using localized low power LDOs or references as power sources for 16+ bit ADCs in measurement or audio applications

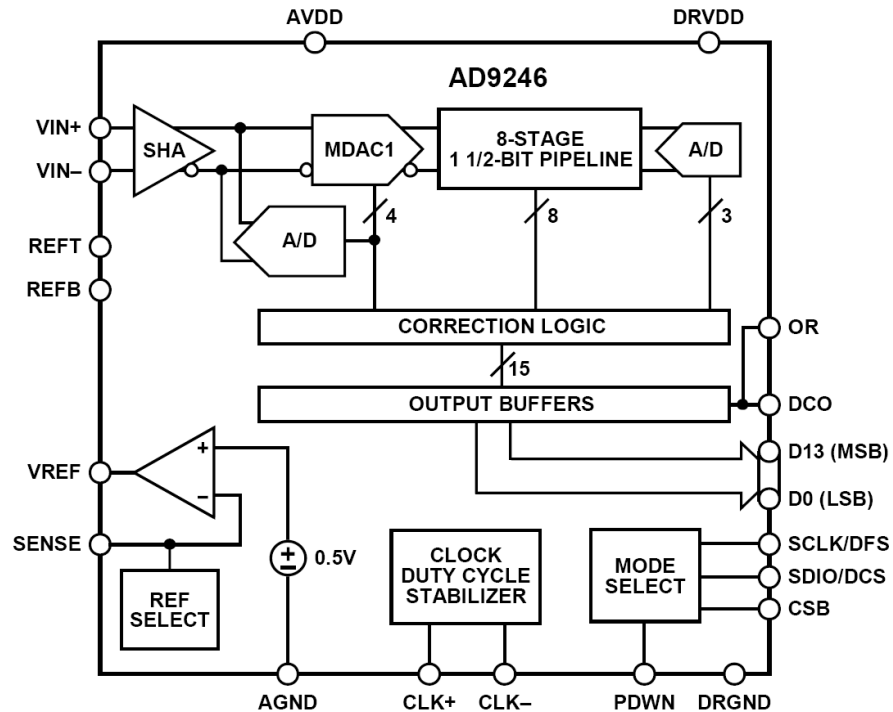
Although dc and 50 Hz or 60 Hz PSR is generally quite good, ac PSR is generally not specified in sigma-delta ADC data sheets.

Because of the high resolution of these devices (up to 24 bits), they should be powered from LDOs rather than risk power supply ripple increasing the overall noise of the converter. This does not usually present a power dissipation problem, because sigma-delta ADCs are typically low power devices.

For audio applications, LDOs should definitely be used to power sigma-delta ADCs in order to minimize the possibility of the ripple frequency mixing with the sampling clock and producing undesirable frequency components within the audio bandwidth.

It should be noted that the addition of LDOs does not eliminate the need for good localized decoupling at the IC power pins. Decoupling is covered in Section 4 of this book.

## AD9246 14-Bit, 125MSPS Pipelined ADC



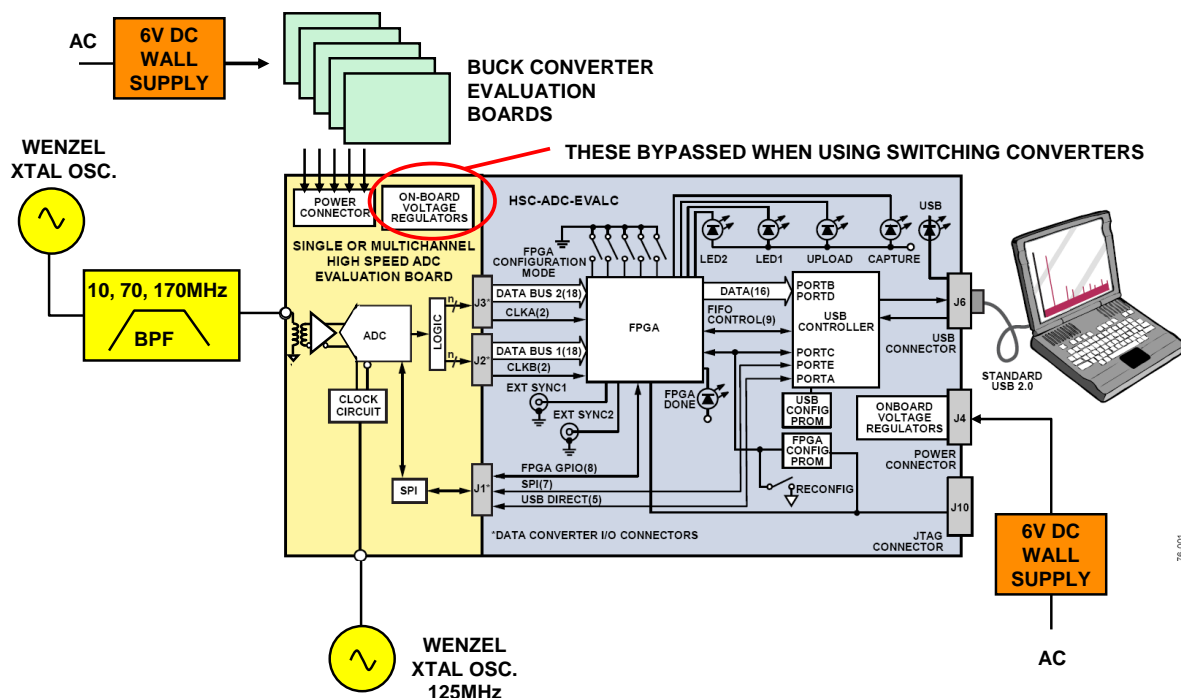
We now look at the PSR characteristics of high speed wide dynamic range pipelined ADCs. This class of ADCs is designed for wide input bandwidth and high SFDR and SNR over a wide range of input frequencies. These converters are often used in IF sampling applications where the input signal is much higher than  $f_s/2$ . Because PSR is rarely specified for this type of ADC, the data must be obtained experimentally.

In order to evaluate the effects of switching supplies on the SFDR and SNR, some experiments were conducted using the AD9246 14-bit, 125MSPS ADC. This is a CMOS ADC with fully differential inputs for both the analog input and the sampling clock input. The part operates on a single 1.8 V analog supply, and a 1.8 V to 3.3 V I/O supply. Power is only 395 mW at a 125 MSPS sampling rate. Outputs are CMOS compatible.

The SFDR is at least 85 dBc and the SNR 71.7 dB for up to 70 MHz inputs. This type of ADC is very sensitive to noise due to layout and power supply and therefore makes a good choice for these experiments.

Most modern high performance pipelined and SAR ADCs have fully differential inputs.

## Test Setup to Evaluate Switching Supply Effect on AD9246 14-Bit, 125MSPS ADC



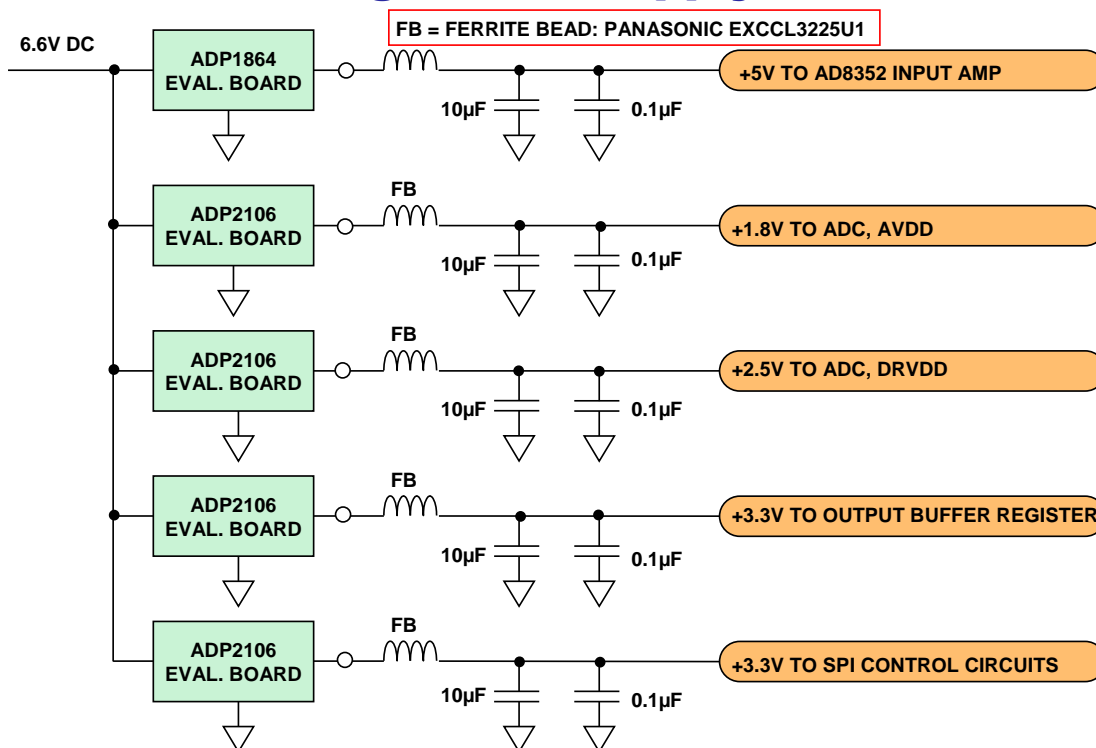
The test setup used for the experiments was a standard ADC evaluation board interfaced to a FIFO (buffer memory) board. The FIFO board interfaces to a computer using the USB port.

This figure shows the standard configuration. The ADC evaluation board is product-specific and contains an input transformer, amplifier, the ADC, clock driver, output buffer logic, and SPI port control logic.

Separate wall mount ac supplies provide the 6 V dc voltage for each board. The ADC evaluation board using LDO point-of-load regulators to supply the voltages to the ADC and the control logic. The FIFO board uses a combination of LDOs and switching converters for its point-of-load power.

The baseline data on SFDR and SNR was first taken using the standard LDOs on the ADC evaluation board. They were then replaced with switching converter evaluation boards, and the experiments were repeated.

## Switching Power Supply Details

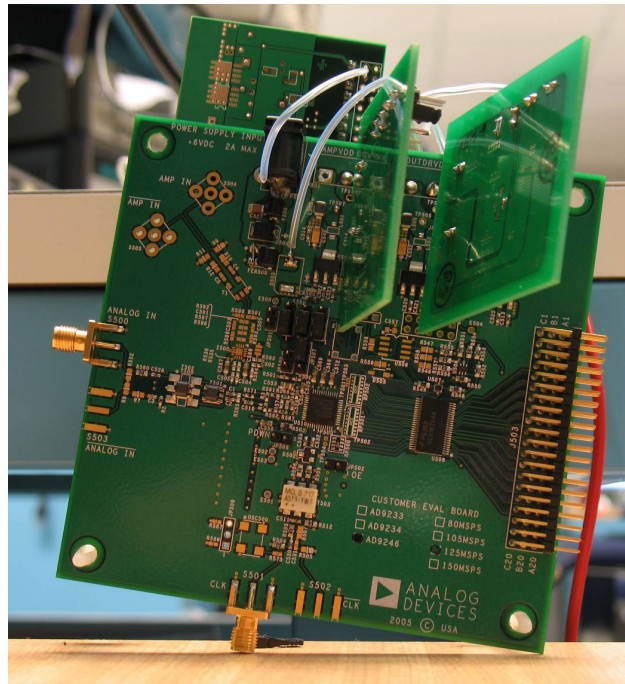


This figure shows how the switching converter evaluation boards were interfaced to the ADC evaluation board voltages. The ferrite beads, 10 µF capacitors, and the 0.1 µF capacitors were part of the ADC evaluation board and located close to the LDOs. In addition, there were the standard recommended localized decoupling capacitors connected close to the power pins of the ADC. The ADC evaluation board external power connector provided a convenient place to connect the switching converter boards and effectively disable the LDOs.

The ferrite bead is a Panasonic EXCCL3225U1 which has an impedance of about 50 Ω from 100 MHz to 1 GHz.

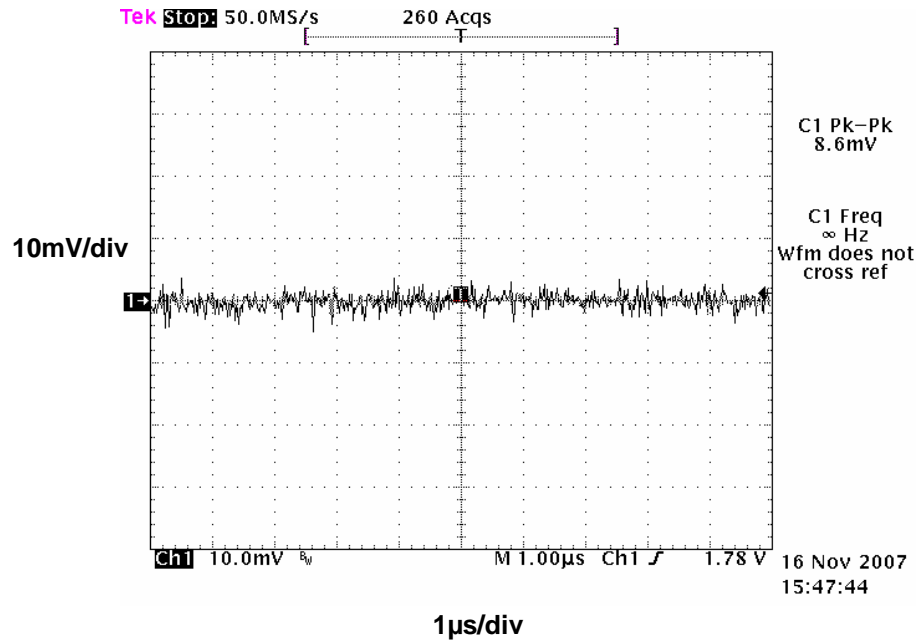
The switching converters were not synchronized to each other.

## **Modified AD9246 Evaluation Board Showing Switching Supply Boards**



This shows a photo of the additional switching supply evaluation boards connected to the ADC evaluation board. No particular care was taken in the interconnections between the supplies and the board in terms of their orientation, although leads were kept as short as practical.

## **ADP2106 Switching Regulator Output Measured at AVDD of AD9246**

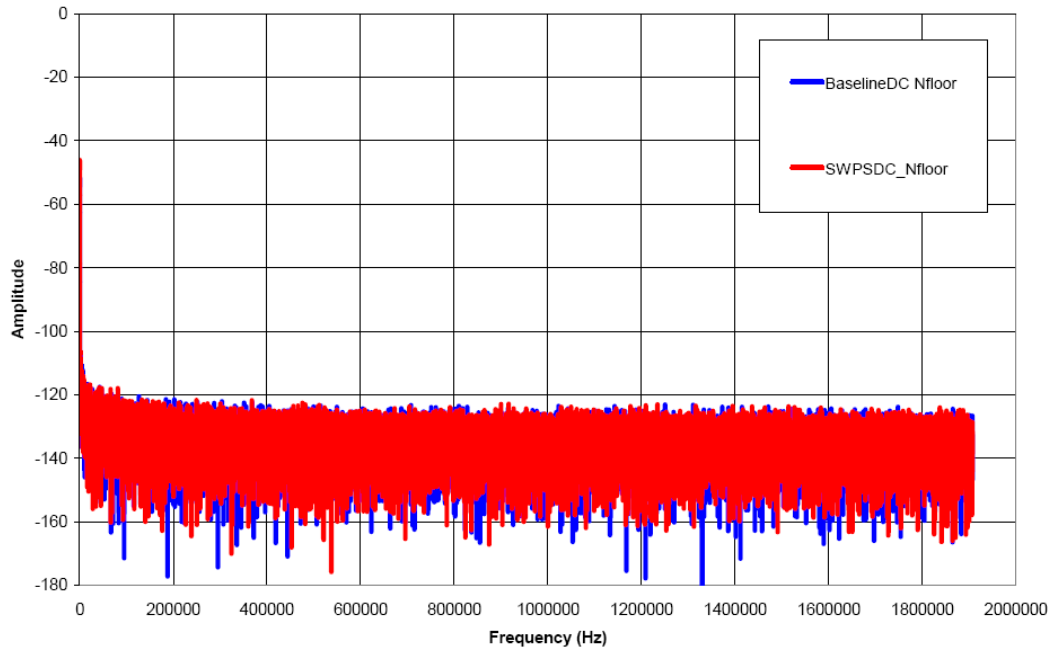


The peak-to-peak ripple was measured at the AVDD pin of the AD9246 and was approximately 10 mV. This measurement was made using all five of the switching regulators connected to the evaluation board. The AVDD pin supplies the power to the analog portion of the AD9246, and is therefore the most sensitive one.

It is difficult to distinguish the ripple components from the noise spikes. The oscilloscope's 20 MHz internal filter was used to remove as much high frequency noise as possible.



## **Noise Floor of ADC for Linear and Switching Supplies with Input Grounded FFT Data Shows Spurs to 2MHz**



This shows an FFT output with the ADC input grounded and the switching supplies connected in place of the LDOs. The sampling rate was 125 MSPS, but the FFT is expanded here to show only the portion up to 2 MHz.

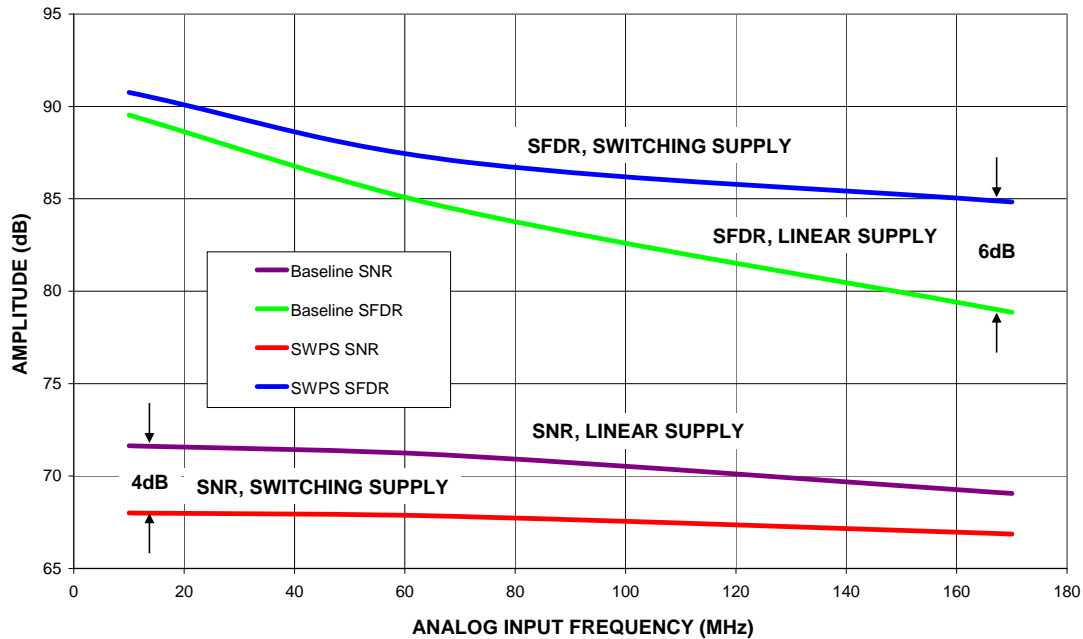
There was little difference between the noise floor using the LDOs or the switching supplies. The overall spur level was approximately 120 dB below full scale.

## Analysis of AD9246 ADC PSR

- ◆ Ripple Free Dynamic Range, RFDR = 120dB from grounded-input FFT plots.
- ◆  $V_{FS\_PP} = 2.0V$
- ◆  $\Delta V_{SS\_PP} = 10mV$
- ◆  $20 \log (2.0/0.01) = 46dB$
- ◆  $PSR = RFDR - 46 = 120 - 46 = 74dB$

We can calculate the approximate PSR of the ADC based on the method previously developed. In this case it works out to be 74 dB.

## **SNR and SFDR of 14-Bit AD9246 for Linear and Switching Supplies, $f_s = 125\text{MSPS}$**



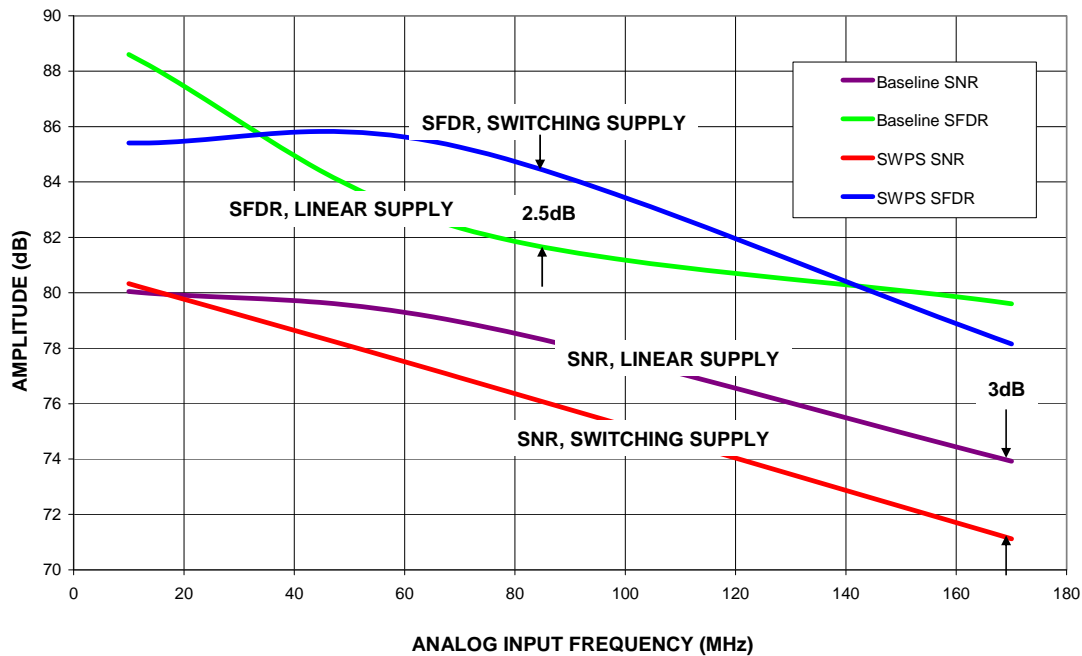
This figure shows the SFDR and the SNR as a function of input frequency for the case of switching supply power and linear supply power.

The SNR was approximately 4 dB worse at low frequencies with the switching supplies. The low frequency (10 MHz) SNR was actually about 68 dB, which does not meet the specified value of 71.9 dB. Although the grounded input FFTs don't indicate significant degradation, the actual SNR of the ADC when stimulated by an ac signal is definitely degraded by the switching supplies.

The effect of power supply noise on SFDR is more difficult to explain, because the switching supply actually improved the SFDR. It has been demonstrated that small amounts of dither noise summed with the analog input signal can improve SFDR in some high performance ADCs. The improvement in SFDR with the switching supply is attributed to this effect. The power supply noise is summed in with the analog signal within the ADC and produces a similar effect. However, under no circumstances should a switching supply be chosen because of the results observed in this particular experiment in anticipation of an SFDR improvement.

It should be noted that you may obtain slightly different results if you conduct these same experiments. The purpose of the experiments is mainly to show the general trend you can expect.

## SNR and SFDR of AD9446 16-Bit, 80MSPS ADC for Linear and Switching Supplies, $f_s = 80\text{MSPS}$



This shows results for a similar experiment conducted with the AD9446 16-bit 80 MSPS pipelined ADC. The ADC has LVDS outputs, and the SNR @ 10 MHz is specified at 79.6 dB.

The vertical scale in this figure is 2 dB/division. The previous figure was 5 dB/division.

In this case, there is no significant change in the SNR for a 10 MHz input signal. The degradation occurs at the higher input frequencies and is approximately 3 dB worse using the switching regulator for a 170 MHz input signal.

The AD9446 16-bit, 80 MSPS ADC appears less sensitive to power supply noise than the 14-bit AD9246 (see previous figure on p. 3.30). This could be because the AD9246 has CMOS outputs, while the AD9446 has LVDS outputs which generate less noise. The digital power supply pins of the CMOS output ADC are more sensitive to noise than those that have LVDS outputs. This is because LVDS logic uses constant current low-level differential switches as opposed to the saturating switches found in CMOS logic.

The maximum variation in the SFDR between the linear and switching supply power is about 2.5 dB, and the curves cross each other. This is within the range of experimental error considering all the variables in the experiment.

## Pipelined ADC PSR Summary

- ◆ No consistency in manufacturer's specifications of PSR for pipelined ADCs. Some specify ripple PSR, but noise rejection may be more important.
- ◆ Experiments show that pipelined ADCs have good PSR for ripple frequency.
- ◆ However, broadband switching noise can decrease SNR. This must be verified by experimentation.
- ◆ Effect of switching noise greater for high input frequencies (IF sampling).
- ◆ With proper filtering, switchers probably ok for 12-bit baseband sampling applications.
- ◆ ADCs with LVDS outputs appear less sensitive to power supply noise than those with CMOS outputs.
- ◆ Experimentation required for 14 or 16 bit applications, or IF sampling.
- ◆ Conservative approach is to use LDOs to power ADCs, or verify performance with switchers by experimentation.

Pipelined ADCs are typically used for sampling rates greater than about 10 MSPS. There are many varieties currently available. Some are designed for baseband operation, and some are designed to handle input signals well above the Nyquist frequency of  $f_s/2$ .

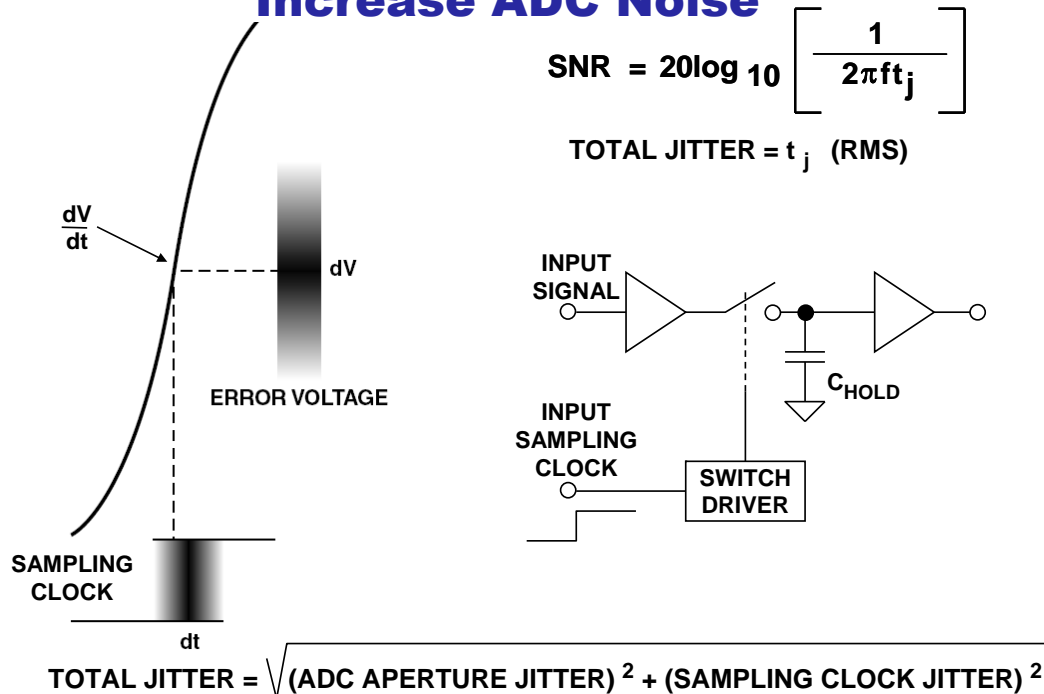
A few have single-ended inputs, but most have differential inputs for both the analog input and sampling clock inputs.

Even though a high speed pipelined ADC may have a PSR specification, it is dangerous to assume that it applies to critical specifications such as SNR or SFDR. The only certain way to determine if a switching supply can be used to power the ADC is to actually run a controlled experiment where the frequency domain results of linear versus switching supplies can be compared.

In some cases, the switching supply noise and ripple may yield acceptable results. The only way to be certain is to try it.

The conservative approach is to use LDOs to power pipelined ADCs unless system efficiency or real estate requirements make this impossible.

## Sampling Clock Jitter and Aperture Jitter Increase ADC Noise



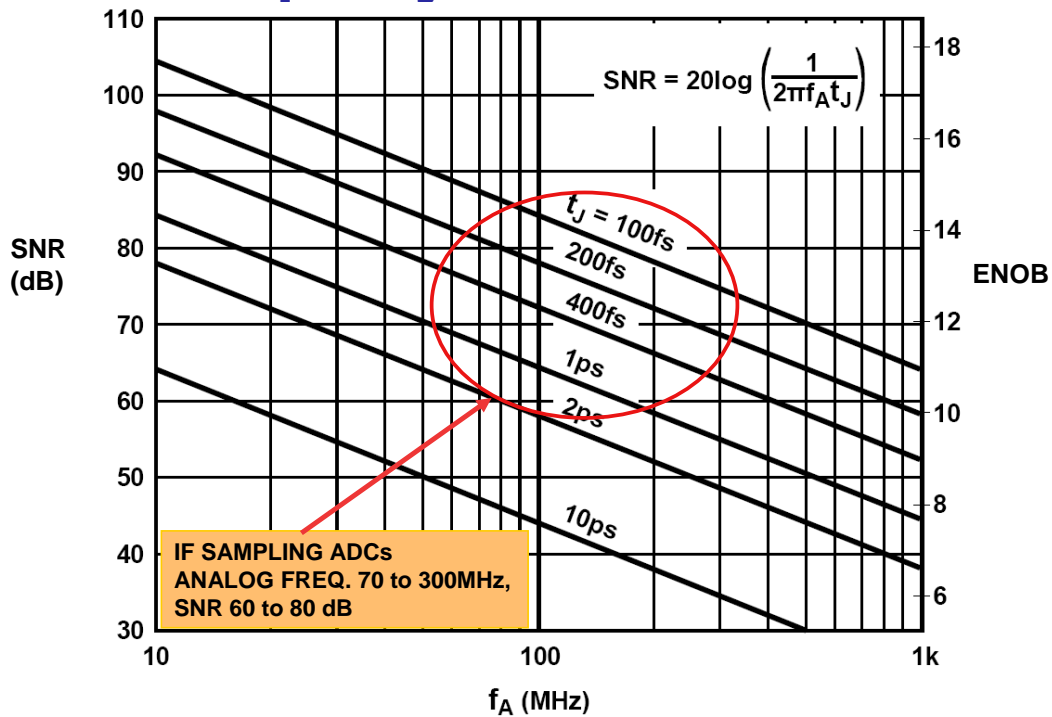
Power supply ripple and noise can affect critical clock generating circuits by increasing the amount of jitter. The ADC sampling clock is especially sensitive. The leading edge determines the instant the ADC takes a sample. The sampling clock jitter translates into a voltage error at the sample-and-hold output as shown here.

The effect is to limit the SNR to a value given by the equation  $SNR = 20 \log(1/2\pi f t_j)$ , where  $f$  is the full-scale analog input frequency, and  $t_j$  is the total jitter. This equation describes the SNR for an ideal ADC of infinite resolution where the only error source is the clock jitter. In practice, the SNR will be worse due to additional error sources.

The ADC aperture jitter is created internally in the sample-and-hold circuit. It combines in a root-sum-square manner with the external clock jitter. In most situations, the external clock jitter dominates.

Most high performance ADCs now use differential sampling clock inputs in order to minimize sensitivity to clock jitter.

## ADC SNR as a Function of Analog Input Frequency and Clock Jitter



This figure shows the theoretical SNR (left side) due to total jitter versus full-scale analog input frequency. The ADC is assumed to have infinite resolution, and the only noise source is that produced by the jitter.

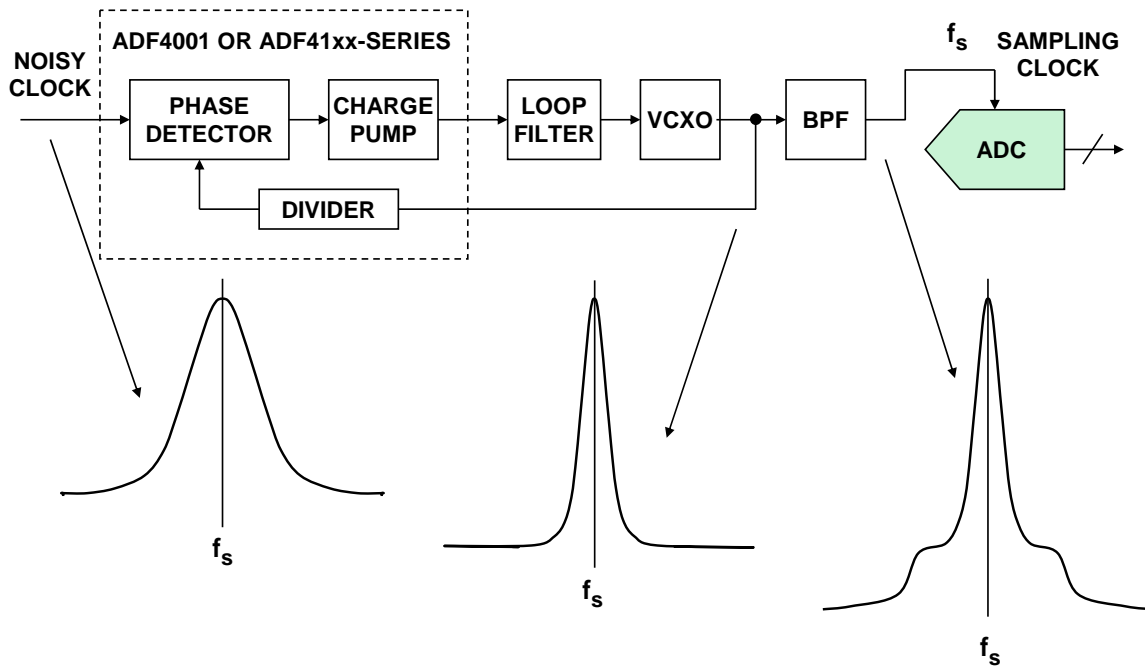
The effective number of bits (ENOB) is shown on the right and is related to SNR by the well known equation,  $SNR = 6.02N + 1.76dB$ , where  $N = ENOB$ .

IF-sampling ADCs typically operate with analog frequencies between 70 MHz and 300 MHz, with system SNR requirements of 60 dB to 80 dB (the circled region). The range of allowable sampling clock jitter for this level of performance is from about 0.1 ps to 2 ps, depending upon the IF frequency and the SNR requirement.

These stringent requirements mean that special care must be taken with the ADC sampling clock, which is often derived from other clocks in the system.

Clock jitter less than 2 ps can only be attained using dedicated crystal controlled oscillators or PLLs with VCXOs.

## Using a Phase-Locked Loop (PLL) and Bandpass Filter to Condition a Noisy Clock Source



Only the highest end systems can afford the dedicated crystal oscillators.

Many systems therefore use a lower-cost combination of a phase-locked loop (PLL) and a VCXO (voltage-controlled crystal oscillator) followed by a bandpass filter to generate a low jitter sampling clock from a noisy system clock.

Circuits such as the one shown in this figure are capable of generating sampling clocks with less than 1 ps rms jitter.

Analog Devices makes a number of PLLs and clock generation and distribution ICs suitable for this function.

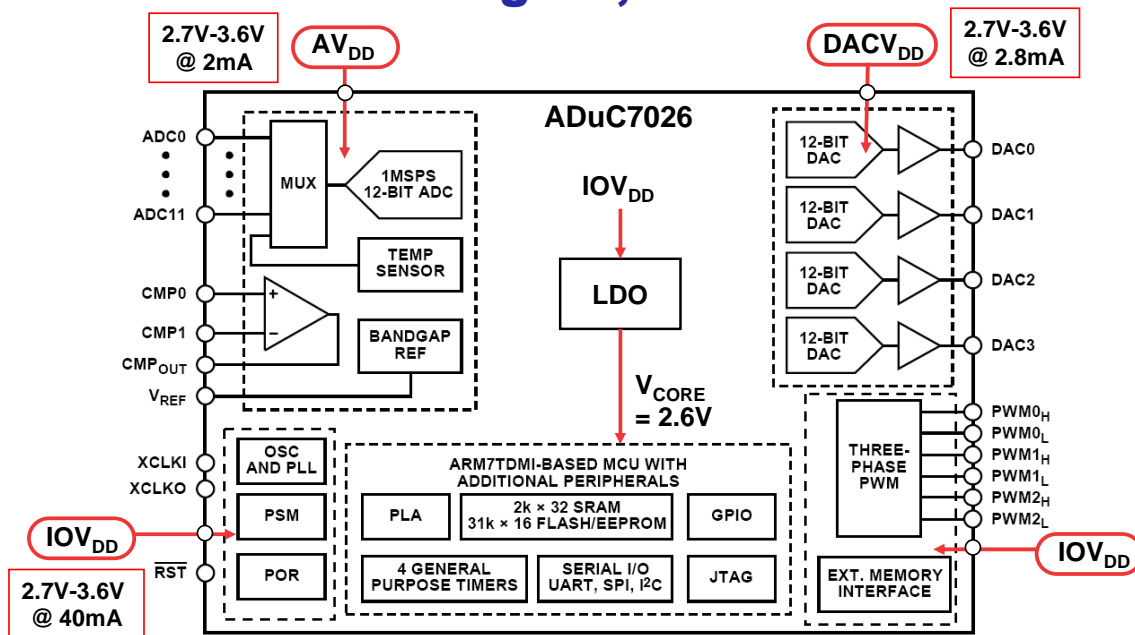
See, [www.analog.com/pll](http://www.analog.com/pll) and [www.analog.com/clocks](http://www.analog.com/clocks) for more information on Analog Device's clock generation products.



## **Powering Precision Analog Microcontrollers**

**[www.analog.com/microcontrollers](http://www.analog.com/microcontrollers)**

## ADuC7026 Precision Analog Microcontroller, with 12-Bit Analog I/O, ARM7TDMI® MCU



The ADuC7019 to ADuC7028 are fully integrated, 1 MSPS, 12-bit data acquisition systems incorporating high performance multichannel ADCs, 16-bit/32-bit MCUs, and Flash/EE memory on a single chip. The ADC consists of up to 12 single-ended inputs. An additional four inputs are available but are multiplexed with the four DAC output pins. The ADC can operate in single-ended or differential input modes. The ADC input voltage is 0 V to  $V_{REF}$  (2.5 V nominal). A low drift band gap reference, temperature sensor, and voltage comparator complete the ADC peripheral set. Depending on the part model, up to four buffered voltage output DACs are available on-chip. The DAC output range is programmable to one of three voltage ranges.

The devices operate from an on-chip oscillator and a PLL generating an internal high frequency clock of 41.78 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an ARM7TDMI, 16-bit/32-bit RISC machine, which offers up to 41 MIPS peak performance. Eight kilobytes of SRAM and 62 kilobytes of nonvolatile Flash/EE memory are provided on-chip. The ARM7TDMI core views all memory and registers as a single linear array. On-chip factory firmware supports in-circuit serial download via the UART or I2C serial interface ports, while nonintrusive emulation is also supported via the JTAG interface. These features are incorporated into a low cost QuickStart™ Development System supporting this MicroConverter family. The parts operate from 2.7 V to 3.6 V and are specified over an industrial temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . When operating at 41.78 MHz, the power dissipation is typically 120 mW. The ADuC7019 to ADuC7028 are available in a variety of memory models and packages.

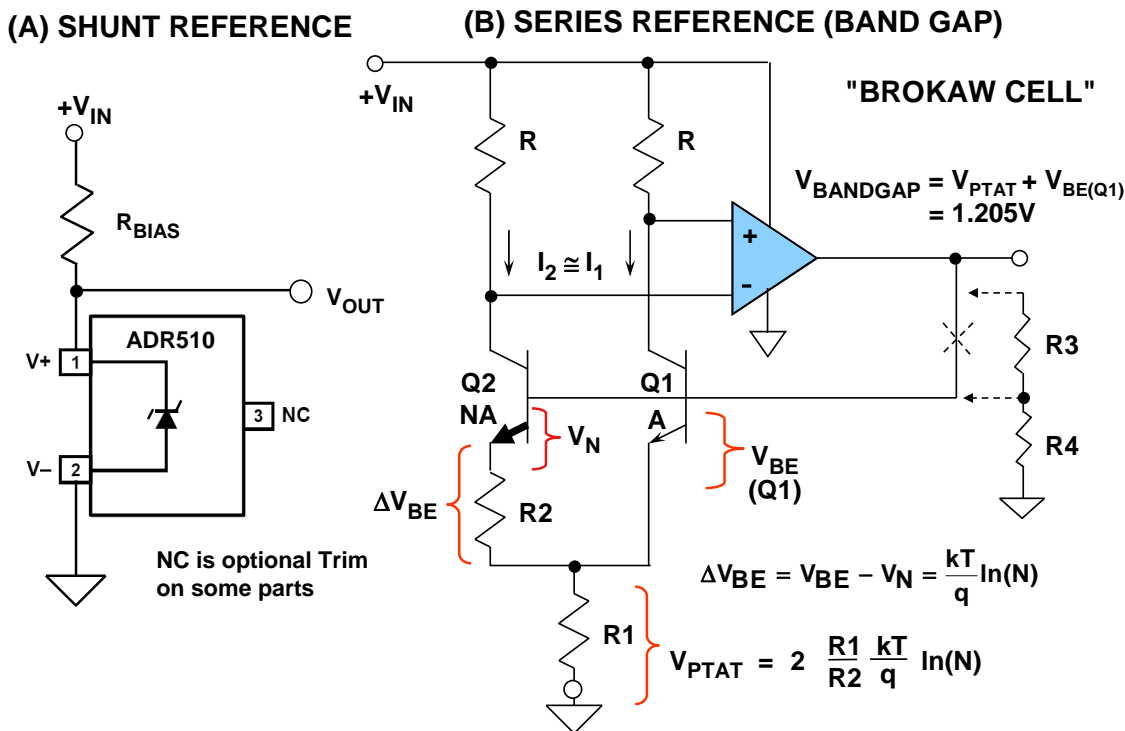
The above block diagram illustrates how power is applied to the part. Analog power is applied to the  $AV_{DD}$  and  $DACV_{DD}$  inputs. The I/O power is applied on the  $IOV_{DD}$  pins, and the internal core voltage of 2.6 V is derived from the  $IOV_{DD}$  voltage using an internal LDO.



# Voltage References

[www.analog.com/references](http://www.analog.com/references)

## Shunt and Series Voltage References



A voltage reference is a low noise, accurate, and well regulated power supply which is designed specifically for data acquisition applications, such as establishing the full-scale input voltage of an ADC or DAC.

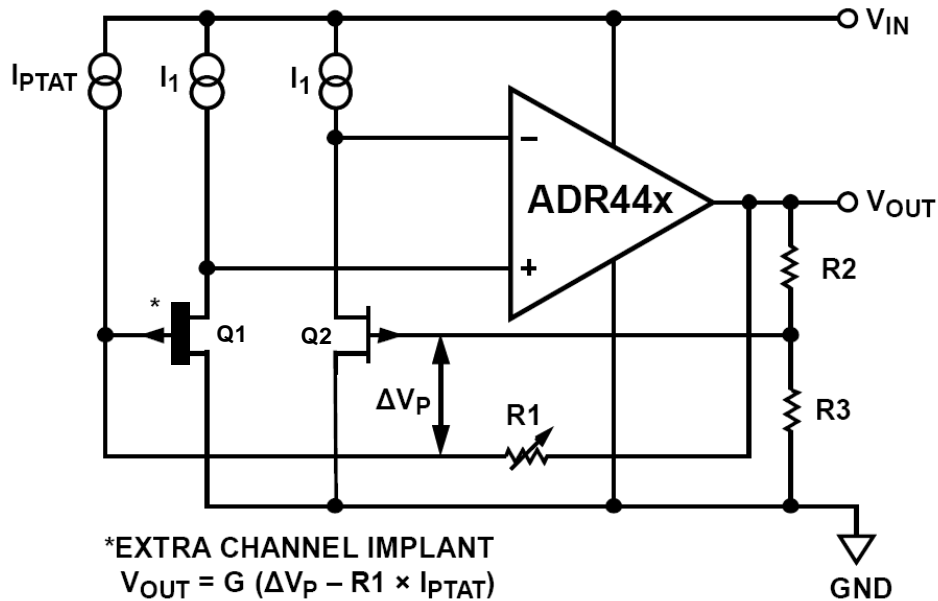
This figure shows two popular types: shunt and series.

The shunt reference in (A) is a two terminal device which essentially acts as a low voltage Zener diode. For example, the ADR510 is a low voltage (1.000 V), precision shunt-mode voltage reference in an ultracompact (3 mm × 3 mm) SOT-23-3 package. The ADR510 features low temperature drift (70 ppm/°C), high accuracy (±0.35%), and ultralow noise (4 μV p-p) performance.

The ADR510 advanced design eliminates the need for an external capacitor, yet it is stable with any capacitive load. The minimum operating current increases from 100 μA to a maximum of 10 mA. This low operating current and ease of use make the ADR510 ideally suited for handheld battery-powered applications.

Both shunt and series references are based on the band gap reference. The circuit in (B) shows a "Brokaw Cell" band gap circuit which forms the basis for many series references. Transistors Q1 and Q2 operate at equal collector currents by virtue of the feedback network. However, the emitter area of Q2 is N times that of Q1. This causes the  $V_{BE}$  drop of Q2 ( $V_N$ ) to be less than that of Q1 by an amount equal to  $(kT/q)\ln(N)$ . The current through  $R2$  is therefore proportional to absolute temperature, PTAT. This current is equal to  $(kT/q)\ln(N)/R2$ . Since an equal current flows through Q1, the sum of the two transistor currents produces a voltage across  $R1$  which is equal to  $2(R1/R2)(kT/q)\ln(N)$ . This voltage is PTAT and is summed with  $V_{BE(Q1)}$  which is complementary to absolute temperature (CTAT), to produce the voltage at the output. When the voltages are scaled (trimming  $R1$  and  $R2$ ) for minimum output TC, the value is approximately equal to the band gap voltage, 1.205 V. Note that the output voltage can then be scaled by simply adding the feedback resistor network shown dotted in the figure.

## XFET® Reference Architecture



The ADR44x series of references uses a new reference generation technique known as XFET (eXtra implanted junction FET). This technique yields a reference with low dropout, good thermal hysteresis, and exceptionally low noise. The core of the XFET reference consists of two junction field-effect transistors (JFETs), one of which has an extra channel implant to raise its pinch-off voltage. By running the two JFETs at the same drain current, the difference in pinch-off voltage can be amplified and used to form a highly stable voltage reference.

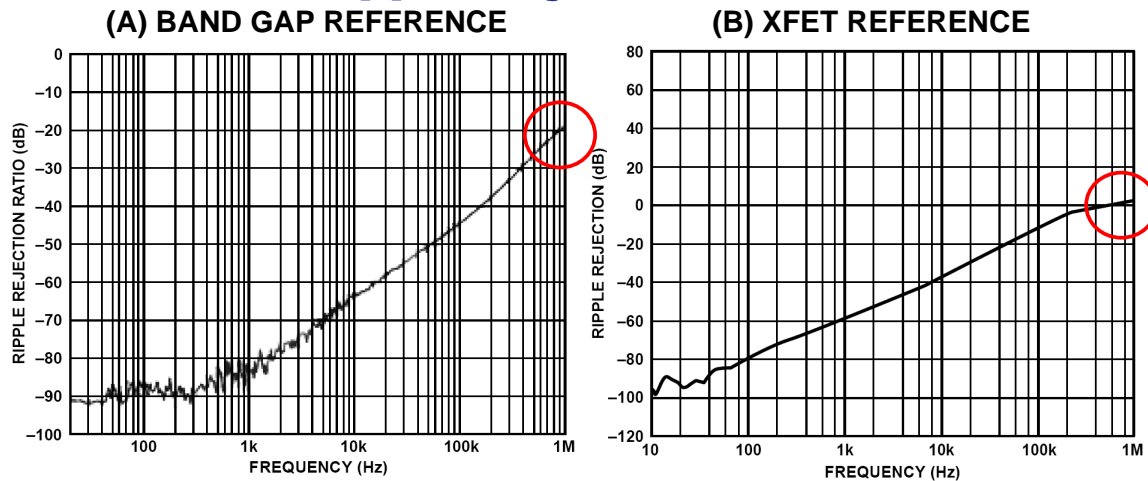
The intrinsic reference voltage is around 0.5 V with a negative temperature coefficient of about  $-120 \text{ ppm}/^\circ\text{C}$ . This slope is essentially proportional to the dielectric constant of silicon, and it can be compensated by adding a correction term generated in the same fashion as the proportional-to-absolute temperature (PTAT) term used to compensate band gap references. The advantage of an XFET reference is its correction term, which is approximately 20 times lower and requires less correction than that of a band gap reference. Because most of the noise of a band gap reference comes from the temperature compensation circuitry, the XFET results in much lower noise. The temperature correction term is provided by a current source with a value designed to be proportional-to-absolute temperature. The general equation is

$$V_{OUT} = G (\Delta V_P - R1 \times I_{PTAT}),$$

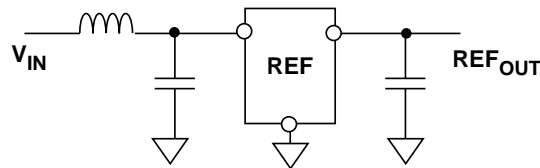
where  $G$  is the gain of the reciprocal of the divider ratio.  $\Delta V_P$  is the difference in pinch-off voltage between the two JFETs.  $I_{PTAT}$  is the positive temperature coefficient correction current.

The reference output voltage of the ADR44x devices is scaled by on-chip adjustment of  $R2$  and  $R3$  to provide different output voltage options.

## Band Gap and XFET Reference Ripple Rejection Ratio



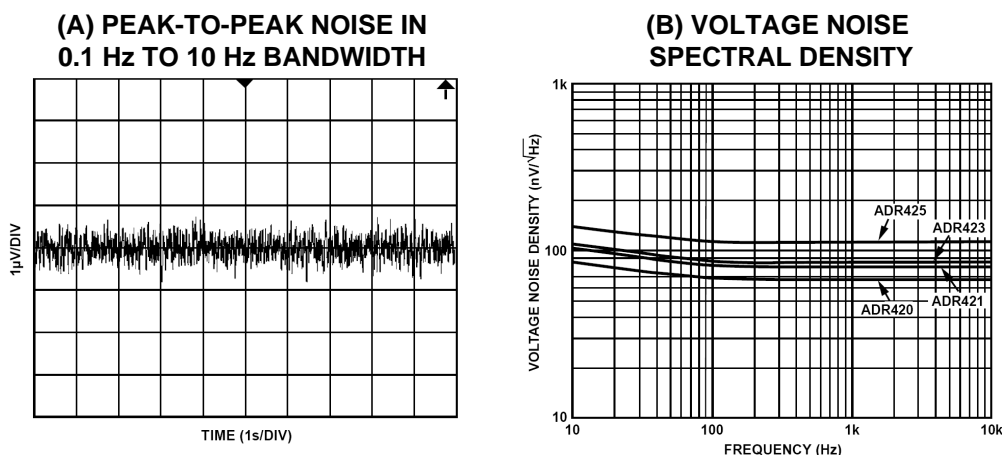
- ◆ Don't count on references to filter power supply ripple!
- ◆ Must use good filtering on the reference input and output



Ripple rejection ratio is shown in this figure for a typical band gap and XFET reference. The 1 MHz ripple rejection of the band gap is 20 dB and the XFET is 0 dB.

For this reason, the input voltage to any reference must be adequately filtered. In most cases, an LC filter is adequate, provided the input capacitor has a low ESR and ESL.

## Voltage Reference Noise



### OTHER WAYS TO SPECIFY NOISE

- ◆ Noise spectral density @ 1 kHz
- ◆ RMS noise measured over 100 kHz bandwidth
- ◆ Must always specify bandwidth!

Voltage reference noise can be specified in a number of ways. The most common is to specify the noise similarly to that of an op amp.

The scope photo in (A) shows the peak-to-peak noise measured in a 0.1 Hz to 10 Hz bandwidth. This standard measurement is important in low frequency high resolution measurement applications.

The plot in (B) shows the traditional rms voltage noise spectral density as a function of frequency. This plot is sometimes referred to as the "spot noise."

It is important to remember that the 0.1 Hz to 10 Hz noise is specified as a peak-to-peak quantity, while the noise spectral density plot is rms.

Note that a noise specification is meaningless unless the bandwidth is also specified. In some cases, reference noise is measured over a 100 kHz bandwidth, but other bandwidths are often used. Sometimes only the noise spectral density (spot noise) at 1 kHz is specified.

Another point to consider is that both the input and output capacitors must also be specified if the noise specification is to be meaningful.



## Reference Noise Requirements for Various System Accuracies (1/2 LSB / 100kHz BW Criteria)

	NOISE DENSITY (nV/ $\sqrt{\text{Hz}}$ ) FOR 10, 5, AND 2.5V FULL-SCALE RANGES		
BITS	10V	5V	2.5V
12	643	322	161
13	322	161	80
14	161	80	40
15	80	40	20
16	40	20	10

- ◆ Criteria:  $V_{N(\text{PP})} < 0.5 \text{ LSB}$ ,  $\text{LSB} = V_{\text{FS}}/2^N$
- ◆ Assume p-p noise  $V_{N(\text{P-P})} \approx 6 \times V_{N(\text{RMS})}$ , calculate  $V_{N(\text{RMS})}$
- ◆ Assume a bandwidth of 100kHz, calculate noise density
- ◆ Noise Density =  $V_{N(\text{RMS})}/\sqrt{100\text{kHz}}$
- ◆ Most references are about 100nV/ $\sqrt{\text{Hz}}$

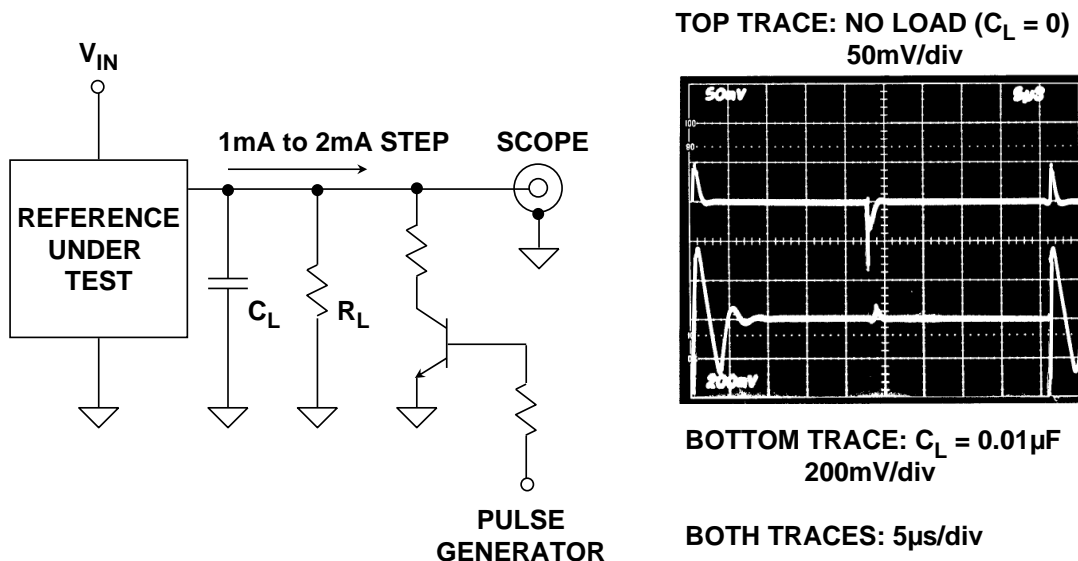
This chart relates noise spectral density to ADC resolution for various signal ranges. It is useful in determining the approximate requirement on the voltage reference noise. It should be noted, however, that further reductions in the rms noise can be achieved with additional filtering. The numbers in the table are calculated as follows:

- The basic criteria is that the peak-to-peak noise should be less than 0.5 least significant bit (LSB).
- An N-bit ADC has  $2^N$  levels. Each level is separated by 1 LSB.
- The LSB value is calculated by dividing the ADC full-scale range,  $V_{\text{REF}}$ , by  $2^N$ .
- One-half LSB is  $2^N \div 2$
- Assume that the peak-to-peak noise is 6 times the rms noise. This is a widely used approximation.
- Divide the LSB value by 12 in order to obtain the approximate rms noise,  $V_{\text{REF}}/(12 \times 2^N)$ .
- Divide the rms noise by the square root of the bandwidth, BW, to get the noise spectral density:

$$E_n \leq \frac{V_{\text{REF}}}{12 \times 2^N \times \sqrt{\text{BW}}}$$

Most voltage references have a noise spectral density of between 50 nV/ $\sqrt{\text{Hz}}$  and 100 nV/ $\sqrt{\text{Hz}}$ . This implies that additional filtering is required for applications requiring greater than approximately 12 bits of resolution.

## References Should Be Stable with Capacitive Loads



As previously discussed, the reference input to an ADC must be heavily decoupled. This means that the reference must be stable with capacitive loads in order to be useful as an ADC reference.

This test set is used to test reference stability by applying a current step to the output and checking for ringing and oscillation. The objective is to simulate the current transients produced by switched capacitor inputs.

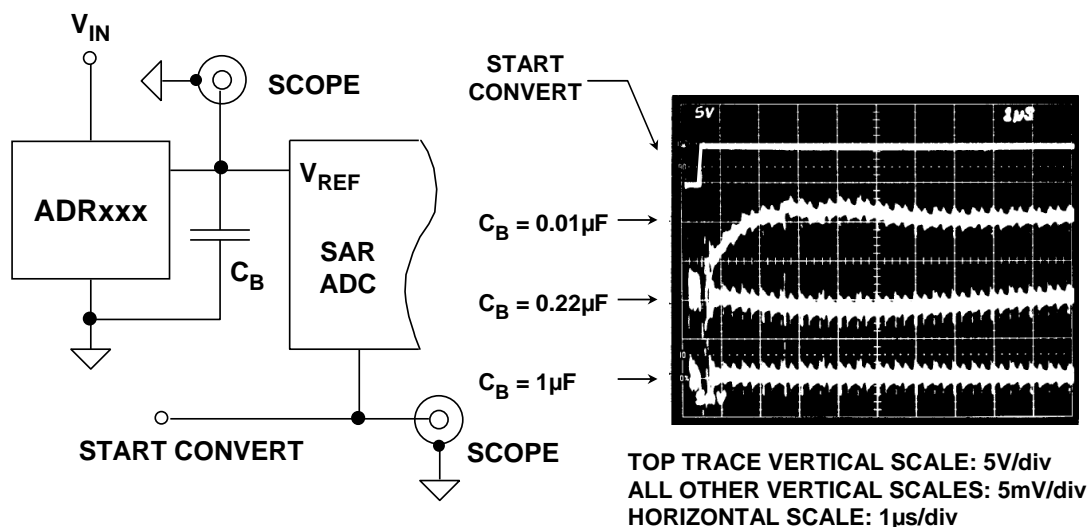
The top trace shows the step response with no capacitive decoupling. The transients are well behaved with no oscillation.

The bottom trace shows the step response with a decoupling capacitor of  $0.01\mu F$ . Note the increased transient amplitude (400 mV) and the ringing.

It is clear that this reference is useless as an ADC or DAC reference because a decoupling capacitor such as the  $0.01\mu F$  used in this test is almost always required. In fact, a larger value ( $1\mu F$  or greater) is preferable and would cause even more instability for this reference.

Modern references should be designed for stability under reasonable decoupling loads, and the data sheet should recommend typical minimum and/or maximum values, and show recommended application circuits.

## External Reference for SAR ADC Requires Energy Storage Capacitor to Prevent Errors



As noted above, reference bypass capacitors are useful when driving the reference inputs of ADCs. This figure illustrates reference voltage settling behavior immediately following the "Start Convert" command for a successive approximation ADC. This particular SAR ADC requires approximately 10 μs to complete the conversion process. A small capacitor (0.01 μF) does not provide sufficient charge storage to keep the reference voltage stable during conversion, and errors will result. As shown by the bottom trace, decoupling with a 1 μF capacitor maintains the reference stability during the entire conversion cycle for accurate results.

Where voltage references are required to drive large capacitances, it is also critically important to realize that their turn-on time will be prolonged. Experimentation may be needed to determine the delay before the reference output reaches full accuracy, but it will certainly be much longer than the time specified on the data sheet for the same reference in a low capacitance loaded state.

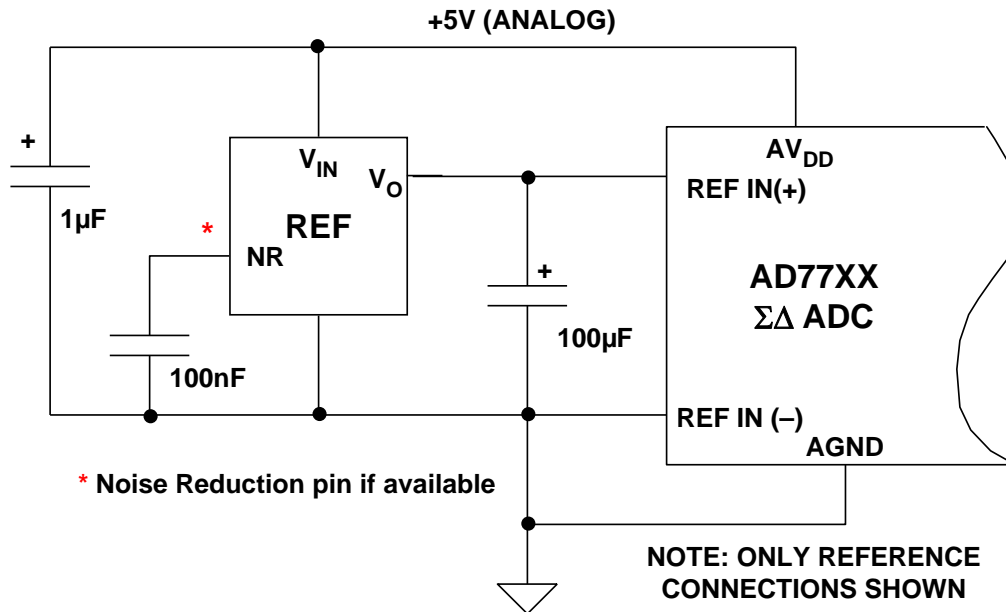
In most cases the data sheet for the SAR ADC gives the required value of the external reference decoupling capacitor for specified performance.

## Reference Temperature Drift Requirements for Various System Accuracies (1/2 LSB Criteria, 100°C Span)

BITS	REQUIRED DRIFT (ppm/°C)	½ LSB WEIGHT (mV) 10, 5, AND 2.5V FULL-SCALE RANGES		
		10V	5V	2.5V
8	19.53	19.53	9.77	4.88
9	9.77	9.77	4.88	2.44
10	4.88	4.88	2.44	1.22
11	2.44	2.44	1.22	0.61
12	1.22	1.22	0.61	0.31
13	0.61	0.61	0.31	0.15
14	0.31	0.31	0.15	0.08
15	0.15	0.15	0.08	0.04
16	0.08	0.08	0.04	0.02

The accuracy of an ADC or DAC can be no better than that of its reference. Reference temperature drift affects full-scale accuracy as shown in this figure. This table shows system resolution and the TC required to maintain 1/2 LSB error over an operating temperature range of 100°C. For example, a TC of about 1 ppm/°C is required to maintain 1/2 LSB error at 12 bits. For smaller operating temperature ranges, the drift requirement will be less. The last three columns of the table show the voltage value of 1/2 LSB for popular full-scale ranges.

## Low Noise Reference Driving a Sigma-Delta ADC



High resolution converters (both sigma-delta and other types) can benefit from recent improvements in IC references, such as lower noise and the ability to drive capacitive loads. Even though many data converters have internal references, the performance of these references is often compromised because of the limitations of the converter process. In such cases, using an external reference rather than the internal one often yields better overall performance.

This figure shows a low noise reference, such as the ADR4xx series, used as the reference for the AD77xx-series ADCs. These references allow a large decoupling capacitor on their outputs thereby minimizing conversion errors due to transients.

There is one possible but yet quite real problem when replacing the internal reference of a converter with a higher precision external one. The converter in question may have been trimmed during manufacture to deliver its specified performance with a relatively inaccurate internal reference. In such a case, using a more accurate external reference with the converter may actually introduce additional gain error! Therefore the data sheet should be carefully checked regarding the use of external references and their possible effect on gain and offset.

## Voltage Reference Summary

<b>BAND GAP</b>	<b>XFET</b>	<b>BURIED ZENER</b>
<b>&lt; 5V Supplies</b>	<b>&lt; 5V Supplies</b>	<b>&gt; 5V Supplies</b>
<b>High Noise @ High Power</b>	<b>Low Noise @ Low Power</b>	<b>Low Noise @ High Power</b>
<b>Fair Drift and Long Term Stability</b>	<b>Excellent Drift and Long Term Stability</b>	<b>Good Drift and Long Term Stability</b>
<b>Fair Thermal Hysteresis</b>	<b>Low Thermal Hysteresis</b>	<b>Fair Thermal Hysteresis</b>

This summarizes the characteristics of the three most popular types of references.

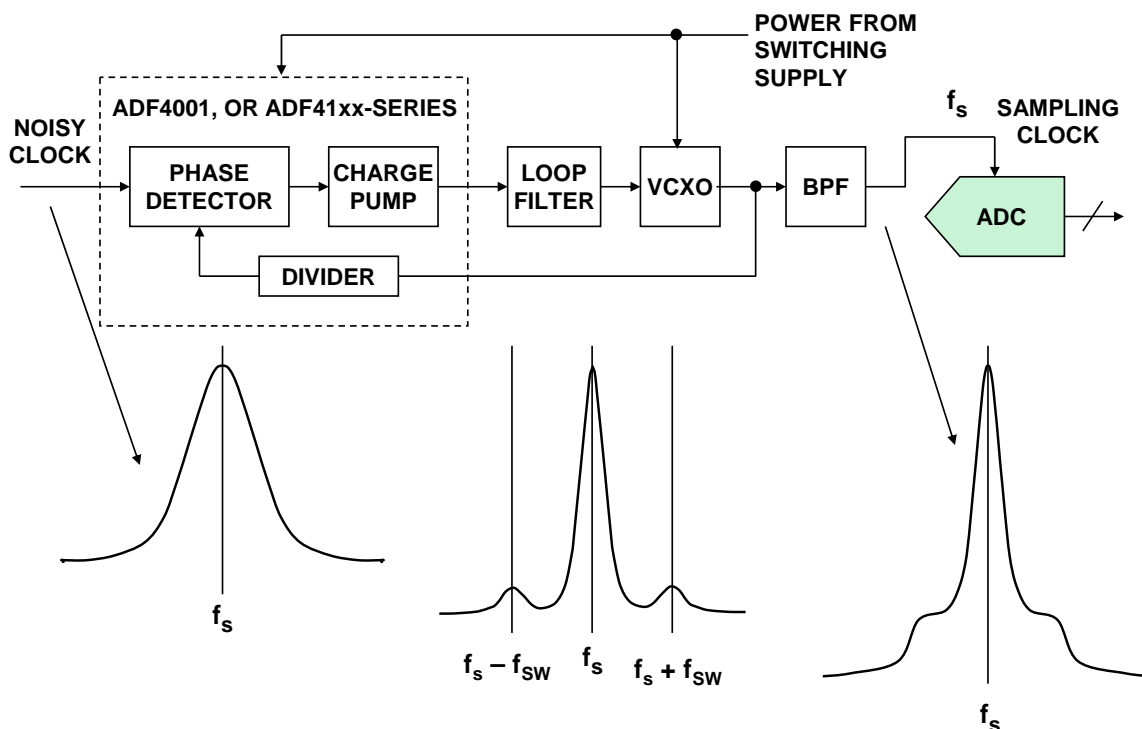
Most modern data converter applications use either the band gap or XFET reference. The buried zener types require supply voltages greater than 5 V and are therefore not relevant to most modern single-supply applications.

The XFET reference series offers the best overall performance for applications greater than 16 bits because of their superior noise and drift characteristics.

## Powering Clock Circuits

[www.analog.com/pll](http://www.analog.com/pll)  
[www.analog.com/clocks](http://www.analog.com/clocks)  
[www.analog.com/dds](http://www.analog.com/dds)

## Power Supply Ripple Modulates PLL Output



Clock generating circuits are more and more critical to a successful system design. Transmitting digital signals at high data rates (sometimes greater than 1 GHz) using CML, LVDS, or other types of fast logic requires low noise supplies to prevent data corruption. An example of this requirement is the Xilinx Virtex-4 FPGA previously discussed in Section 1, where the manufacturer specifically recommends LDOs for powering the high-speed I/O circuits.

As previously discussed, sampling clocks to ADCs must also be low noise and low jitter in order to achieve the required SNR performance.

The two most popular methods for frequency synthesis are phase-locked-loops (PLLs) and direct digital synthesis (DDS). In many cases, a combination of the two offers the optimum solution. PLLs can generate frequencies well into the GHz range, but don't have the tuning flexibility of DDS. Since the upper frequency output of DDS systems is limited by the output DAC clock rate, DDSes generally are limited to an output frequency of approximately 500 MHz. It is common for DDSes to drive PLLs, a combination which takes advantage of both techniques.

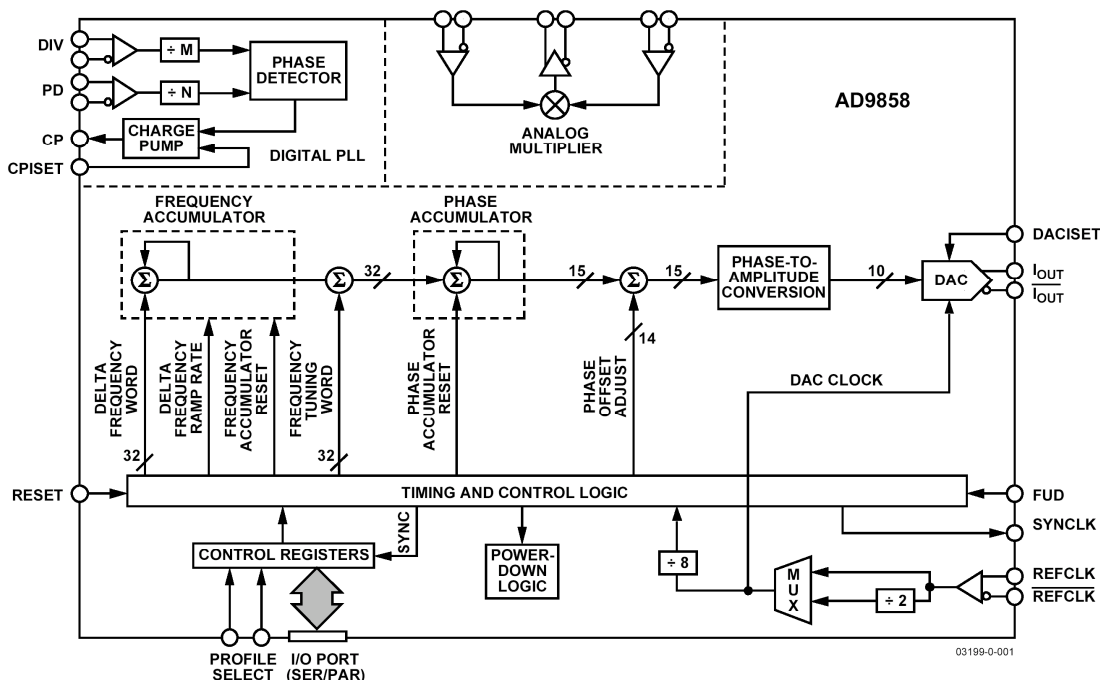
Dedicated crystal oscillators provide the lowest noise and phase jitter, however they are expensive. Many systems therefore use a lower-cost combination of a phase-locked loop (PLL) and a VCXO (voltage-controlled crystal oscillator) followed by a bandpass filter to generate a low jitter sampling clock from a noisy system clock.

Analog Devices makes a number of PLLs and clock generation and distribution ICs suitable for this function.

Switching supply and noise modulate the fundamental output frequency as shown in the figure. This sensitivity of PLLs and DDSes is rarely specified on data sheets. Experiments were conducted on a representative DDS system to explore this sensitivity.



## AD9858 1GSPS DDS with Phase Detector and Analog Multiplier



This figure shows a block diagram of one of Analog Devices' DDS ICs. The AD9858 is a direct digital synthesizer (DDS) featuring a 10-bit DAC operating up to 1 GSPS. The AD9858 uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sine wave at up to 400 MHz.

The AD9858 is designed to provide fast frequency hopping and fine tuning resolution (32-bit frequency tuning word). The frequency tuning and control words are loaded into the AD9858 via parallel (8-bit) or serial loading formats.

The AD9858 contains an integrated charge pump (CP) and phase frequency detector (PFD) for synthesis applications requiring the combination of a high speed DDS along with phase-locked loop (PLL) functions.

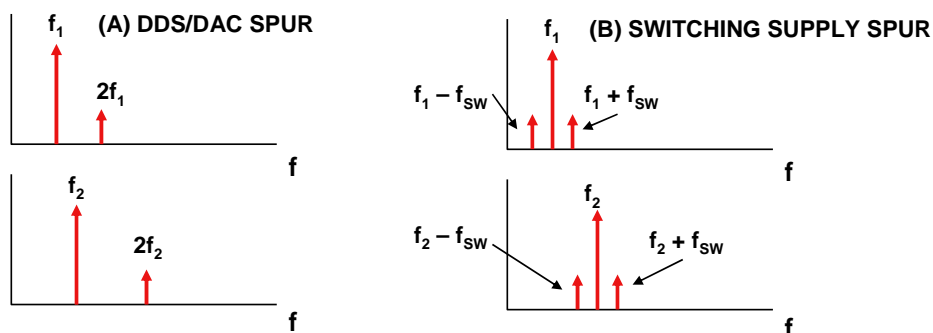
Another benefit of the DDS approach to frequency synthesis is the ability to very accurately and reliably inject phase offsets. 14 bits of phase control allow fine adjustments to ~0.022 degrees as well as supporting phase hopping in the same way that frequency hopping is supported.

Note that a second accumulator has been included in the DDS architecture. Shown here specifically driving the frequency tuning word, this enables a very easy and well controlled method for sweeping across a range of frequencies rather than holding at, or jumping between, specific frequencies. The newest DDS chips allow the second accumulator to drive the phase and amplitude control functions of the DDS as well, so that either of these may be swept instead of the frequency.

An analog mixer is also provided on-chip for applications requiring the combination of a DDS, PLL, and mixer, such as frequency translation loops, tuners, and so on. The AD9858 also features a divide-by-two on the clock input, allowing the external clock to be as high as 2 GHz.

## Determining If Spurs Are Coming from Power Supply in DAC/DDS Systems

- ◆ (A) If the frequency offset of a spur relative to the fundamental output frequency changes as the output frequency changes, then the DDS DAC is probably the source of the spur.
- ◆ (B) If frequency offset of spur relative to the fundamental frequency output remains unchanged as the output frequency changes, then the spur is not coming from the DDS DAC. This would be the case of a power supply ripple component modulating the DDS output, or modulation on the reference clock.



Spurious free dynamic range (SFDR) is a key specification for a DDS system output, but determining the source of unwanted spurs can sometimes be a daunting task unless some fundamentals are understood.

The most common source of spurs are those created by the DDS DAC itself. Manufacturers go to great lengths to design low glitch high SFDR DACs, and typically specify SFDR as a function of output frequency, output amplitude, DAC update rate, etc.

Spurs can also occur if the output frequency is an exact submultiple of the DAC update rate. This is a well known effect which is caused when quantization noise becomes correlated with the output frequency rather than remaining randomly distributed over the Nyquist bandwidth.

The most common type of output spur is created by the non-linearity of the DAC and its switches and occurs at harmonics of the fundamental output frequency. This is increasingly true as the output frequency is increased to its upper limit, which is usually about 1/3 the update rate.

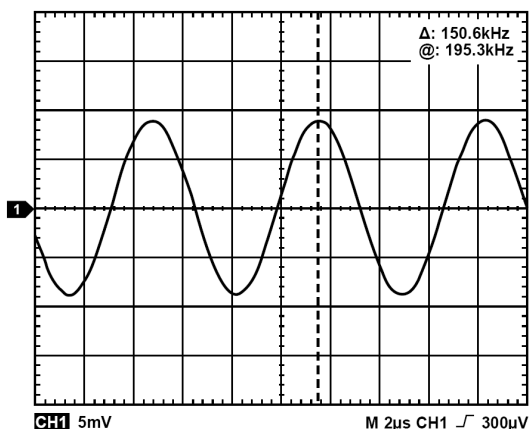
The offset of these spurs from the fundamental output frequency changes as the output frequency changes as shown in (A) for the second harmonic.

On the other hand, the ripple frequency of a power supply modulates the fundamental output frequency producing spurs which are a constant offset from the fundamental as in (B). The offset remains constant regardless of the fundamental output frequency. The separation of the spurs from the fundamental is equal to the switching frequency, making them fairly easy to identify. There can be other spurs, but these close-in spurs are generally the largest ones.

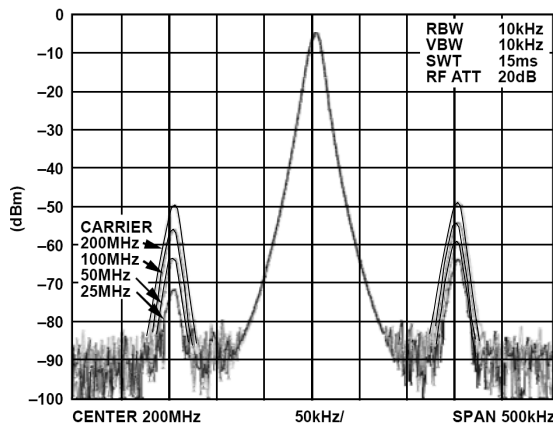
It should be noted that spurs on the DDS reference clock produce the same effect as ripple spurs on the power supply, so care must be taken that the reference clock is clean. If the internal DDS PLL is enabled, then it can produce spurs which are offset from the carrier frequency by an amount equal to the PLL reference frequency.

## Superposition of Four DDS Output Carriers with 150kHz AM Modulation on AVDD Power Supply

**+1.8V POWER SUPPLY MODULATION:**  
16mV (p-p), ( $\pm 0.44\%$ ), 150kHz



**AD9959 DDS OUTPUT SPECTRUM:**  
 $f_s = 500\text{MSPS}$ ,  $f_{OUT} = 25\text{MHz}$ , 50MHz,  
100MHz, 200MHz (Superimposed)



This shows an actual DDS output for four output frequencies, where the 1.8 V power supply is modulated by a 150 kHz, 16 mV p-p sinewave. The DAC update rate is 500 MSPS.

The 25 MHz, 50 MHz, 100 MHz, and 200 MHz outputs are superimposed on each other. In each case the 150 kHz sidebands appear at a constant offset of 150 kHz from the fundamental carrier frequency. (See Reference 1.)

Notice that the frequency offset of the spur on the output remains fixed in frequency offset to all four of the carrier frequencies. However, the amplitude of the spur follows a  $20 \log(x)$  change where  $x$  is the ratio of the frequency of the DDS carrier output to the reference clock frequency. In other words, each time the carrier frequency is doubled, the spur amplitude increases by 6 dB. (See Reference 2.)

This data was taken with the internal DDS PLL disabled and driving the reference clock input directly from a 500 MHz low noise spectrally pure oscillator.

### REFERENCES:

1. David Brandon, "Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)," Application Note AN-927, Analog Devices, 2007. Available at [www.analog.com](http://www.analog.com).
2. Paul Smith, "Little Known Characteristics of Phase Noise," Application Note AN-741, Analog Devices, 2004. Available at [www.analog.com](http://www.analog.com).

## DDS RFDR/PSR Analysis (Very Approximate)

- ◆ RFDR = 50 dB from previous photo.
- ◆  $V_{FS\_PP} = 1.0V$  (Typical DAC output voltage into resistive load)
- ◆  $\Delta V_{SS\_PP} = 16mV$  @ 150kHz (from previous figure)
- ◆  $PSR = RFDR - 20\log(V_{FS\_PP}/\Delta V_{SS\_PP}) = 50 - 35.9 = 14.1dB$
  
- ◆ Frequency synthesis ICs (PLLs, DDSes) do not generally have PSR specifications.
- ◆ Power supply ripple frequency spurs can be distinguished from DDS DAC spurs, but it may be too late when you find them.
  
- ◆ Summary: Should always use well filtered LDO to supply PLLs and DDS unless experimentation and/or manufacturer's data indicates otherwise.

We can perform a very crude calculation which gives the PSR of the DDS system in terms of the spur amplitude.

From the spectral outputs, the worst case spur occurs for a 200 MHz carrier frequency, and its amplitude is approximately 50 dB below full-scale. Therefore, assume that RFDR = 50 dB.

The full-scale voltage output of the DDS DAC is approximately 1 V p-p into a 50  $\Omega$  load. Therefore  $V_{FS\_PP} = 1.0$  V.

The 150 kHz power supply ripple injected onto the 1.8 V supply has an amplitude of approximately 16 mV.

The PSR is then calculated from our previous formula,

$$PSR = RFDR - 20\log(V_{FS\_PP} / \Delta V_{SS\_PP}) = 14.1 \text{ dB.}$$

To summarize, power supply ripple spurs can be distinguished from DDS DAC spurs, but it may be too late when you find them.

The conservative approach is to always use well filtered LDOs to supply PLLs and DDSes unless experimentation and/or manufacturer's data indicates otherwise.

## Reducing Power Supply Noise by Bulk Filtering

We will discuss power supply filtering in two parts. The first is known as bulk filtering, and generally occurs directly at the output of the switching supply. The input and output capacitors are included in this topic, as well as additional filtering components which may be required.

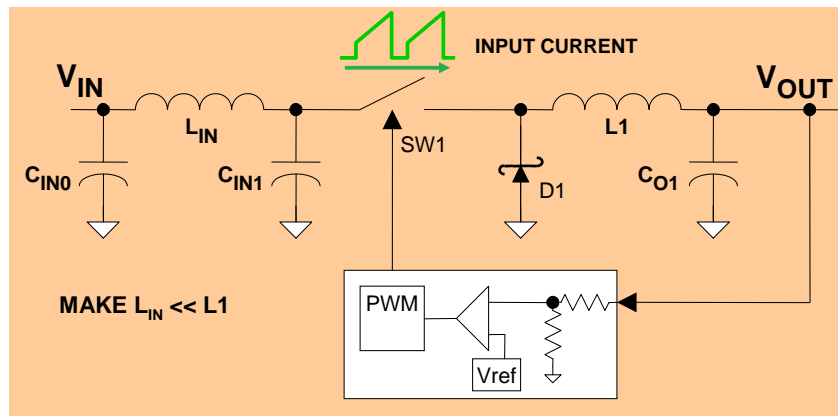
The second type of filtering is the localized decoupling which must be applied to each IC power pin. Proper localized decoupling is mandatory for modern ICs to function properly.

Another method to reduce power supply ripple and noise is to use an LDO following the switching supply. This method must be used with caution, however, because LDOs generally have poor PSR at switching frequencies.

The final method to reduce the effects of power supply ripple and noise is to physically separate the power supply from the rest of the circuits. This can usually be achieved with proper PC board layout.

## Buck Converter with Input Filter

- ◆ Buck switchers have discontinuous input current
- ◆ Input filter can be used to reduce conducted noise
- ◆ Input filter can prevent beat frequencies between switchers
- ◆ Typical  $L_{IN}$  is much smaller than  $L1$

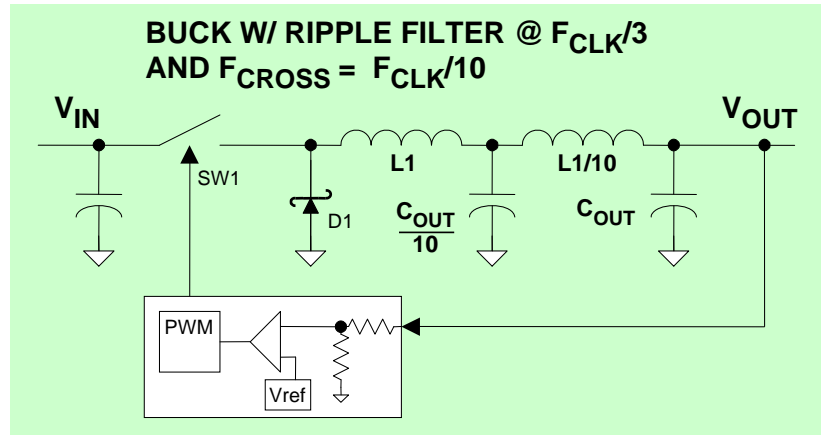


A buck converter has a discontinuous input current which may require additional filtering in order to reduce conducted EMI and prevent crosstalk. In the above circuit, the input filter inductor  $L_{IN}$  is generally much smaller than  $L1$ .

Multiple buck converters used without input filters can produce a beat frequency ripple at the input and output of each converter. For this reason, multiple switchers often use a common synchronized clock.

## Buck Converter with Output Ripple Filter

- ◆ Output filter can be added to reduce ripple and spikes
- ◆ Good layout is required to get the full benefit
- ◆ Closing the feedback loop around the filter is tricky
- ◆ Putting the filter outside the feedback loops hurts transient response
- ◆ Ripple out can be reduced to < 1mV p-p



The buck converter has a continuous output ripple current, but further filtering may be required. A single LC filter may be limited by both component and PCB trace ESR and ESL.

Increasing the value of the inductor L1 will reduce the ripple current and the output ripple voltage, but also increases the size and cost of the circuit. Large values for L1 can degrade the step response. In many cases, an additional LC filter as shown in this figure can reduce the output voltage ripple with less performance degradation and at lower cost. However, closing the feedback loop around the filter can be tricky because of the additional poles.

The value for L1 is chosen as a normal part of the design of the buck converter.  $C_{OUT}$  and L1 produce a double pole at  $1/[2\pi\sqrt{(L1 \cdot C_{OUT})}]$ . The additional pole created by L1/10 and  $C_{OUT}/10$  is positioned at  $F_{CLK}/3$ . This will attenuate the ripple by 10 dB.

The loop unity gain frequency ( $F_{CROSS}$ ) should be set  $< F_{CLK}/10$  to provide a fast loop that is stable. Details get into compensation methods and loop control modes and some more mathematics.

As an example, assume that  $F_{CLK} = 1$  MHz,  $L1 = 10$   $\mu$ H,  $L1/10 = 1$   $\mu$ H. We have the following equation:

$$\frac{F_{CLK}}{3} = \frac{1}{2\pi\sqrt{\frac{L1}{10} \times \frac{C_{OUT}}{10}}}$$

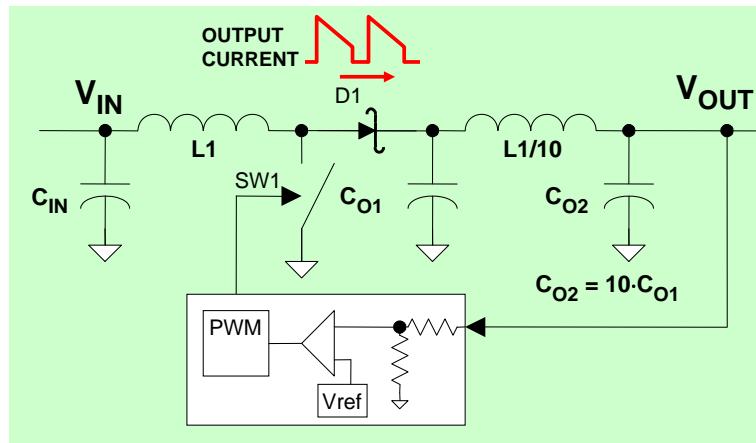
Substituting the above values for  $F_{CLK}$  and L1 and solving for  $C_{OUT}$ , we obtain  $C_{OUT} = 2.3$   $\mu$ F and  $C_{OUT}/10 = 0.23$   $\mu$ F.

Proper layout in conjunction with the use of output filtering as shown here can reduce the peak-to-peak output ripple to less than 1 mV.

Note that simply adding an LC to reduce ripple will affect compensation and step response. Better step response and loop stability fall out of the "big L little C followed by little L big C" implementation described above. If step response is not an issue, then the filter can be placed outside the feedback loop. In this case the voltage dropped across the external ESR of the inductor will not be included in the feedback correction.

## Boost Converter with Output Ripple Filter

- ◆ Ripple and switching spikes are often too high, especially when powering analog circuits
- ◆ Output filter reduces capacitance needed for  $C_{O1}$
- ◆ Output filter reduces RMS ripple spec for  $C_{O2}$
- ◆ Total size/cost may actually decrease



The boost converter has continuous input current, but discontinuous output current. The output ripple and spikes are therefore more troublesome than for the buck converter, especially if powering analog circuits.

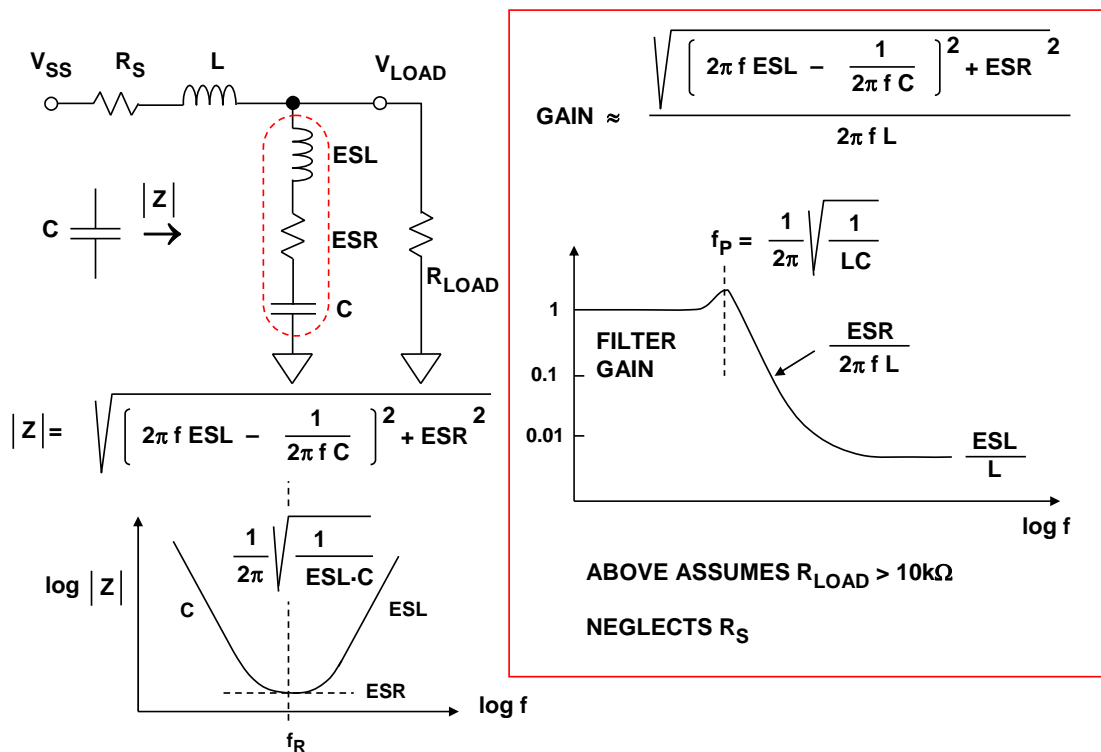
Although the output ripple and noise can be reduced by adding more and more low ESR bulk capacitance, an attractive alternative is to add an additional stage of filtering. This shows an additional LC filter on the output, consisting of  $L1/10$  and  $C_{O2}$ . The additional filter reduces the capacitance required for  $C_{O1}$  and reduces the rms ripple requirement for  $C_{O2}$ . After optimizing the filter, the total size and cost of the overall circuit may actually decrease than by simply increasing  $C_{O1}$ .

$C_{O2}$  is generally  $C_{O1} \times 10$  or more.  $C_{O1}$  should be low ESR (ceramic) to remove the spikes and limit ripple.  $C_{O2}$  is usually much larger to provide the bulk needed for step response and loop stability.

Reversing the capacitor placement will degrade stability and load step response.



## LC Filter Attenuation Approximation



Generalized LC filter design can be implemented using a SPICE-based simulation program such as National Instruments Multisim™. Analog Devices offers a special edition of Multisim that is free and can be downloaded. The free version is similar to the full-featured version except for the number of nodes and components allowed.

This simple LC filter model includes the most important parasitics associated with the inductor and the capacitor.

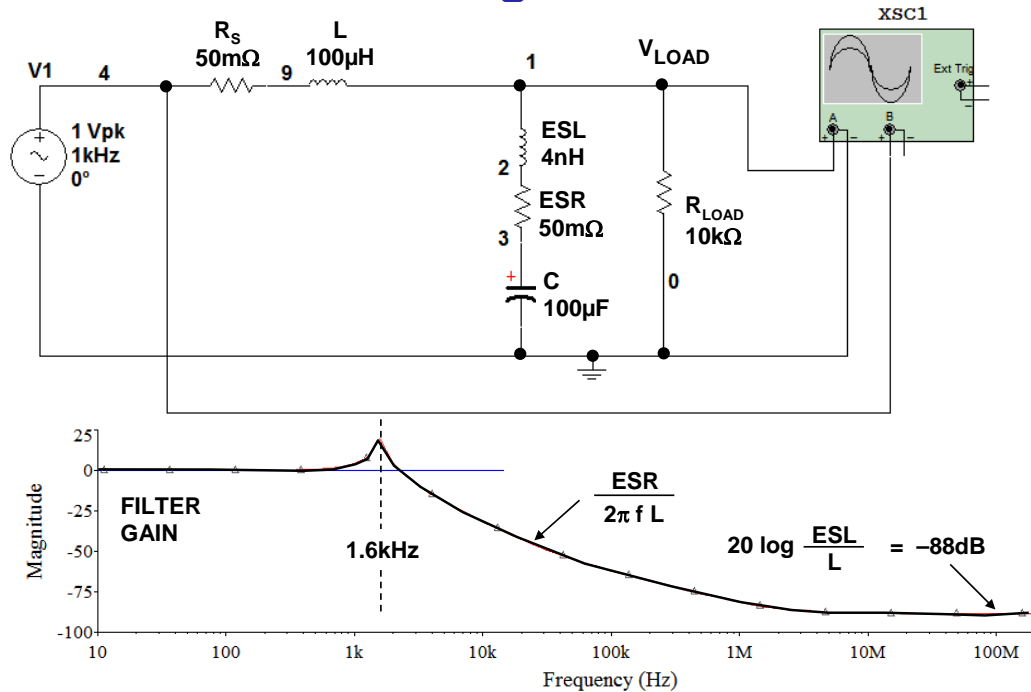
The impedance of the capacitor is shown on the left. At low frequency, the capacitance determines the impedance. As the frequency approaches the self-resonant frequency of the capacitor, the ESR of the capacitor dominates. At higher frequencies, the capacitor ESL dominates.

The "peak" in the overall filter gain plot occurs when the input inductor,  $L$ , resonates with the capacitor,  $C$ . If desired, the peaking can be eliminated by adding an additional resistance in series with the inductor. The generalized frequency response of this network is shown on the right.

After the resonant peak, the gain drops at a rate of 6 dB/octave due to the inductor,  $L$ . It then flattens out at a value approximately equal to  $ESL/L$ . This curve neglects the effects of the load resistance and the ESR and parasitic capacitance of the inductor.

The load impedance is chosen to be 10 kΩ, representing that of a single low power IC. In a practical simulation, the load resistance should be chosen so that the load current approximates that of the IC.

## Simulated Gain of LC Network Using NI Multisim Analog Devices Edition



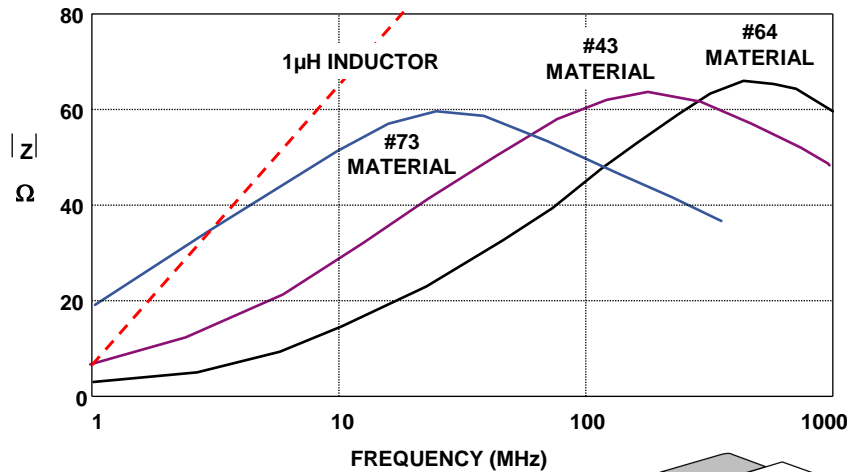
This simple LC filter model includes the most important parasitics associated with the inductor and the capacitor. The Multisim model is shown for an inductor of 100 μH (ESR = 50 mΩ) and a 100 μF capacitor (ESR = 50 mΩ, ESL = 4 nH). The ESR and ESL values are typical of an electrolytic capacitor. The load is simulated with a 10 kΩ resistor.

The "peak" in the overall filter gain plot occurs at approximately 1.6 kHz when the input 100 μH inductor resonates with the 100 μF capacitor. If desired, the peaking can be eliminated by adding an additional resistance in series with the inductor.

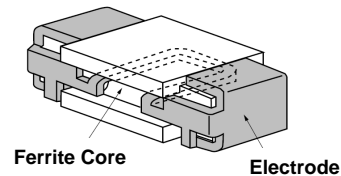
Simple LC filters such as this one can be easily simulated using Multisim. It is important to include the PC board parasitics, especially the parasitic inductance and resistance associated with vias and interconnections. If designed properly, this type of filter should be capable of providing at least 60 dB of attenuation to switching power supply noise and ripple.

More detailed discussions of parasitics associated with inductors and capacitors can be found in Section 4.

## Ferrite Bead Impedance Compared to a 1 $\mu$ H Inductor



Courtesy: Fair-Rite Products Corp, Wallkill, NY  
([www.fair-rite.com](http://www.fair-rite.com))



Ferrite beads are often used in power supply filters, and they are available in small surface mount packages. Unlike inductors, the ferrite bead impedance is mostly resistive at the higher frequencies as shown here for several types of ferrite materials. Ferrite beads are equivalent to lossy inductors. When used in a simple LC filter, the effective Q of the bead is low enough so that there is usually no peaking.

The dc resistance of a ferrite bead is very low (10 to 50 m $\Omega$  typical), and care must be taken that the current through the bead does not exceed the maximum specified rated saturation current. If it does, the ferrite bead becomes a short circuit. Beads with maximum currents up to several amps are available in surface mount packages.

The figure shows the impedance of a 1  $\mu$ H inductor as the dotted line compared to the bead impedances. If high attenuation is required using an LC filter, then the inductor is a better choice.

## **Reducing Ripple and Noise by Localized Decoupling and Filtering**

## What Is Proper Localized Decoupling?

- ◆ A large electrolytic capacitor (typ. 10  $\mu\text{F}$  – 100  $\mu\text{F}$ ) no more than 2 in. away from the chip.
  - The purpose of this capacitor is to be a reservoir of charge to supply the instantaneous charge requirements of the circuits locally so the charge need not come through the inductance of the power trace.
- ◆ A smaller cap (typ. 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ ) as physically close to the power pins of the chip as is possible.
  - The purpose of this capacitor is to short the high frequency noise away from the chip.
- ◆ Optionally a small ferrite bead or inductor in series with the supply pin.
  - Localizes the noise in the system.
  - Keeps external high frequency noise from the IC.
  - Keeps internally generated noise from propagating to the rest of the system.

As previously stated, the electrolytic type large value capacitors are used as local charge reservoirs. This means that the instantaneous current requirements do not have to be met by the power supply, which may be located an appreciable distance away with a considerable amount of inductance and resistance in the line.

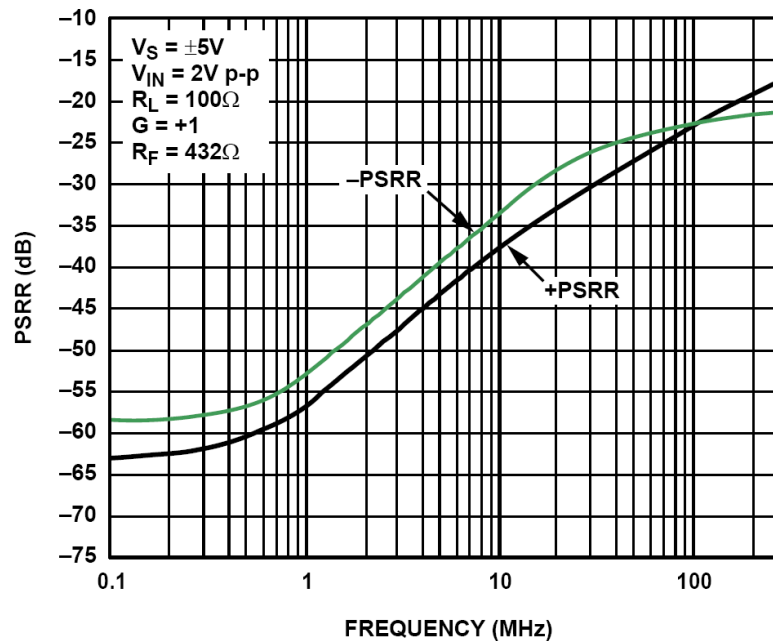
Smaller value capacitors are used to short the high frequency interference away from the chip. Relevant parameters here are low equivalent series inductance (ESL) and equivalent series resistance (ESR). Quite often multilayer ceramics are excellent choices for these applications. At frequencies above the resonant frequency of the capacitor, the ESL dominates, so smaller packages generally give lower inductance at the expense of smaller values of capacitance.

Ferrites (nonconductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are useful for decoupling in power supply filters. At low frequencies (<100 kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100 kHz, ferrites become resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, dc bias current, number of turns, size, shape, and temperature.

The ferrite beads or inductors may not always be necessary, but they will add extra high frequency noise isolation and decoupling, which is often desirable. Possible caveats here would be to verify that the beads never saturate, especially in circuits that consume high currents. When a ferrite saturates it becomes nonlinear and loses its filtering properties.

Note that some ferrites, even before full saturation occurs, can be nonlinear; so if a power stage is required to operate with a low distortion output, this should also be checked in a prototype.

## Power Supply Rejection Ratio vs. Frequency for the AD8000 1.5GHz Op Amp



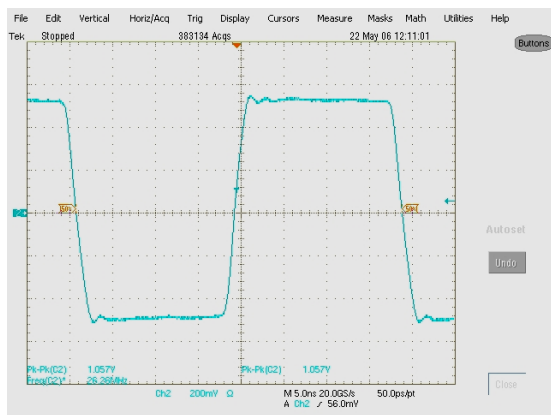
Why is decoupling necessary?

This graph shows how the power supply rejection (PSR) of an amplifier varies with frequency. At high frequencies there is little isolation between the power supply pin and the amplifier output. Therefore, a large portion of any high frequency energy on the power line will couple to the output directly. So it is necessary to keep this high frequency energy from entering the chip in the first place. This is done by using a small ceramic capacitor to short the high frequency signals away from the chip.

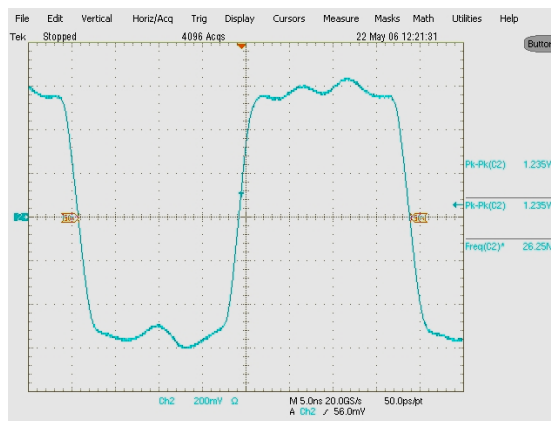
Power supply rejection of data converters has been discussed earlier in this section.

Another aspect to decoupling is the lower frequency interference. Here we use larger electrolytic capacitors.

## Effects of Decoupling on Performance of the AD8000 Op Amp



**PROPER DECOUPLING**



**NO DECOUPLING**

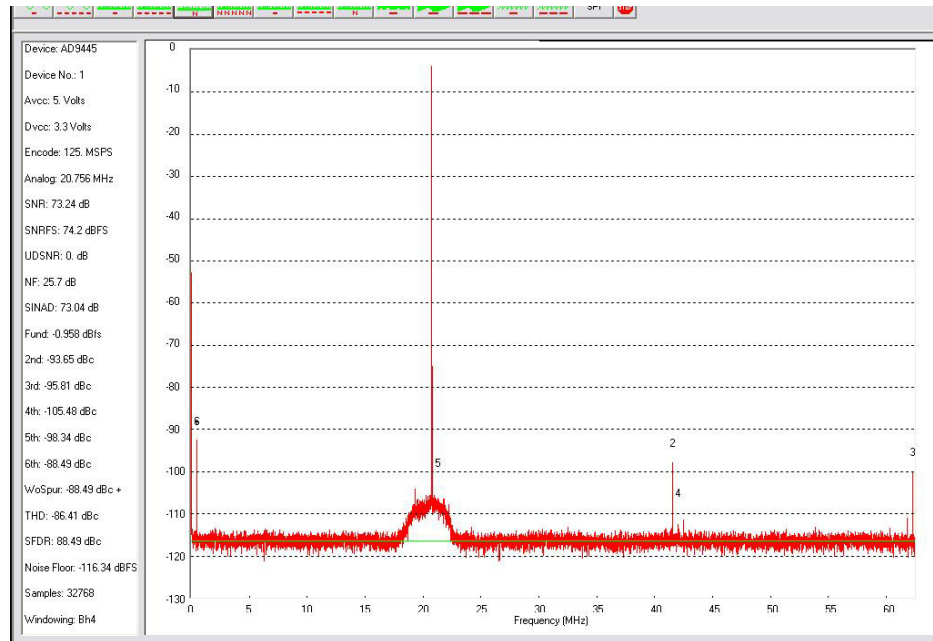
Here is an example of what could happen to the response of an op amp with no decoupling.

Both of the oscilloscope graphs were taken on the same evaluation board.

The difference is that on the right the decoupling capacitors were removed.

Other than that, everything remained the same. In this case the device was an AD8000, a 1.5 GHz high speed current feedback op amp, but the effect will occur in most any high speed IC.

## **FFT Plot for the AD9445 Evaluation Board with Proper Decoupling**



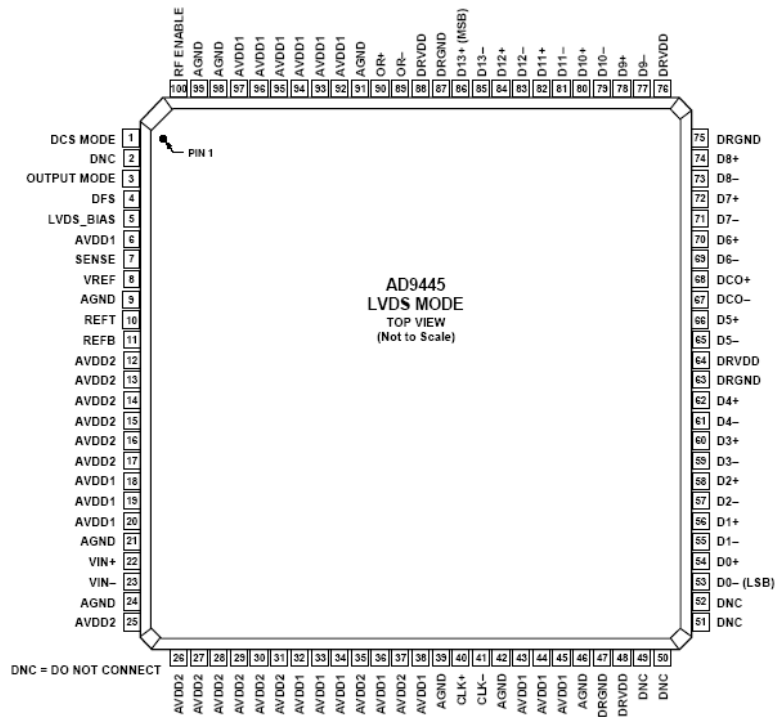
We will now examine the effect of proper and improper decoupling on a high performance data converter, the AD9445 14-bit, 105 MSPS/125 MSPS ADC.

A converter will typically not have a PSR specification, and proper decoupling is very important.

Here is the FFT output of a properly designed circuit. In this case, we are using the evaluation board for the AD9445. Note the clean spectrum.



## AD9445 Pinout Diagram



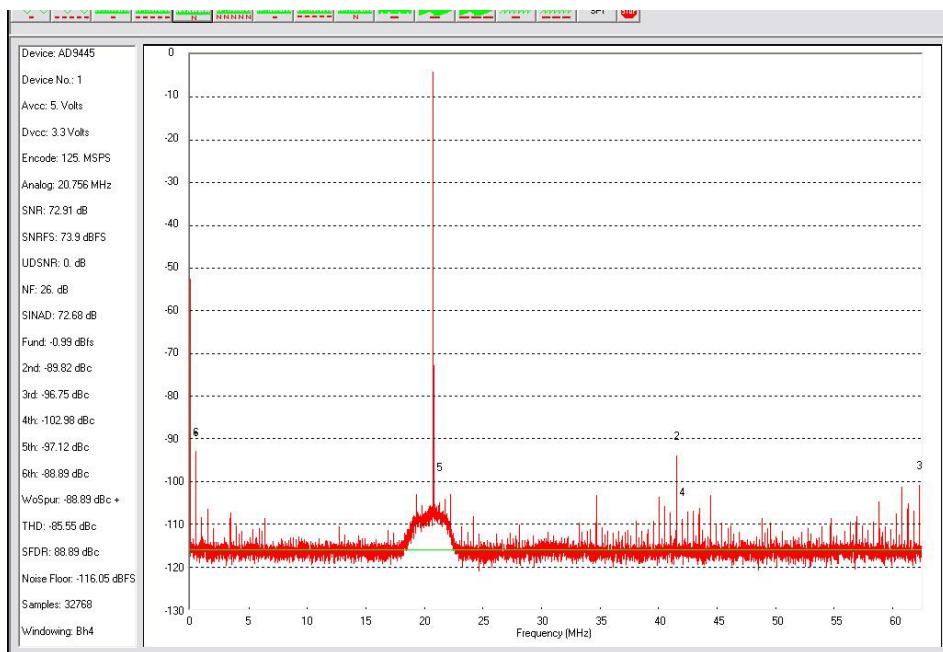
This is the pinout of the AD9445. Note that there are multiple power and ground pins. This is done to lower the impedance of the power supply (pins in parallel).

There are 33 analog power pins. 18 pins are connected to AVDD1 (which is  $+3.3\text{ V} \pm 5\%$ ) and 15 pins are connected to AVDD2 (which is  $+5\text{ V} \pm 5\%$ ). There are four DVDD (which is  $+5\text{ V} \pm 5\%$ ) pins.

On the evaluation board used in this experiment, each power pin has a decoupling cap.

In addition, there are several  $10\text{ }\mu\text{F}$  electrolytic capacitors as well.

## **FFT Plot for an AD9445 Evaluation Board with Caps Removed from the Analog Supply**



Here is the spectrum with the decoupling caps removed from the analog supply.

Note the increase in high frequency spurious signals, as well as some intermodulation products (lower frequency components).

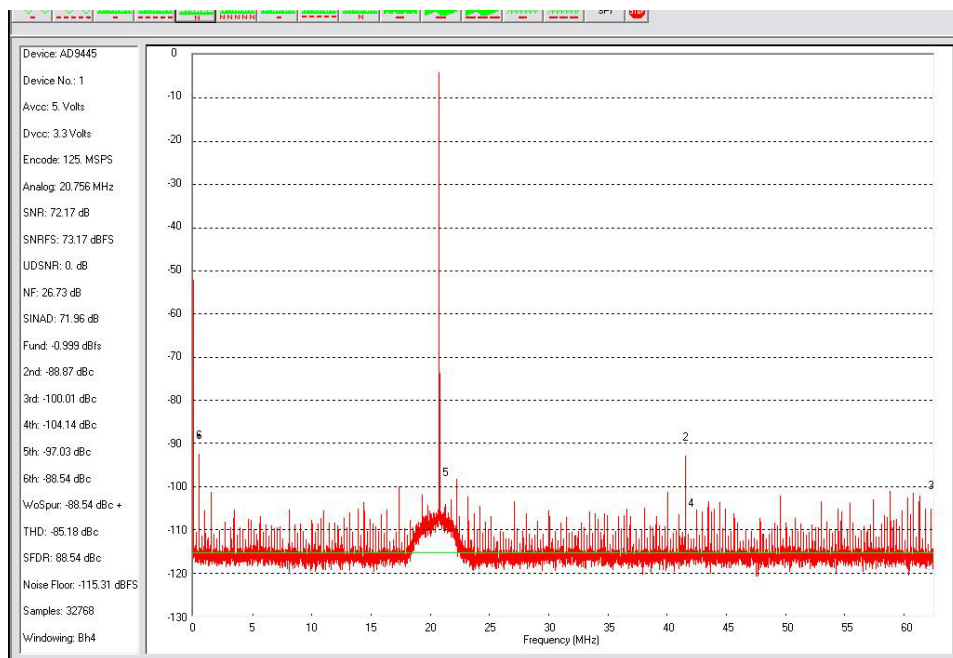
The SNR of the signal has obviously degenerated.

The only difference between this figure and the last is removal of the decoupling capacitors.

Again we used the AD9445 evaluation board as a test vehicle.

In the experiment, the capacitors were removed one at a time. Initially, the SNR degradation was approximately proportional to the number of capacitors removed. With fewer and fewer remaining decoupling capacitors, the SNR curve began to flatten (similar to an amplifier's 1 dB compression point).

## **FFT Plot for an AD9445 Evaluation Board with Caps Removed from the Digital Supply**



Here is the result of removing the decoupling caps from the digital supply. Again note the increase in spurs. Also note the frequency distribution of the spurs.

Not only do these spurs occur at high frequencies, but across the spectrum.

This experiment was run with the LVDS version of the converter.

We can assume that the CMOS version would be worse because non-saturating current mode LVDS logic is less noisy than saturating CMOS logic.

More information on PC board design techniques can be found in the following three references:

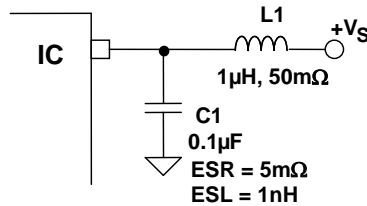
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Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273 Chapter 9. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410, Chapter 9.

Walt Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN: 0-916550-26-5, Chapter 7. Also available as *Op Amp Applications Handbook*, Elsevier-Newnes, 2004, ISBN: 0-7506-7844-5, Chapter 7.

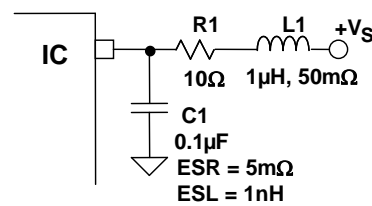
Hank Zumbahlen, *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034, Chapter 12.

## Resonant Circuit Formed by Power Supply Decoupling Network

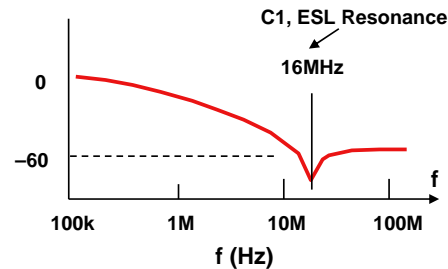
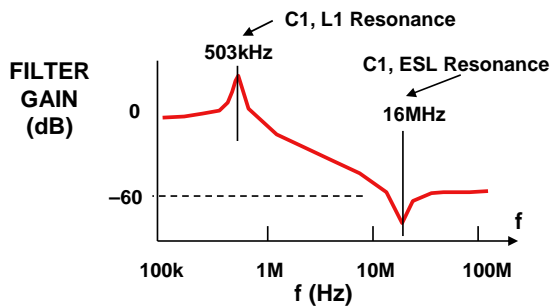


(A) EQUIVALENT DECOUPLED POWER LINE CIRCUIT RESONATES AT:

$$f = \frac{1}{2\pi\sqrt{LC}}$$



(B) SMALL SERIES RESISTANCE CLOSE TO IC REDUCES Q.  
OR USE FERRITE BEAD INSTEAD OF INDUCTOR



An inductor in series or parallel with a capacitor forms a resonant, or "tuned," circuit, whose key feature is that it shows marked change in impedance over a small range of frequency. Just how sharp the effect is depends on the relative Q (quality factor) of the tuned circuit. The Q of a resonant circuit is a measure of its reactance to its resistance.

$$Q = 2\pi f (L/R)$$

If stray inductance and capacitance in a circuit forms a tuned circuit, then that tuned circuit may be excited by signals in the circuit, and ring at its resonant frequency.

Most ceramic capacitors from 0.01  $\mu$ F to 0.1  $\mu$ F will self-resonate well above a few MHz. For example, a 0.1  $\mu$ F capacitor with an ESL of 1 nH resonates at 16 MHz. However in the circuit shown on the left (A), the 0.1 $\mu$ F capacitor and 1  $\mu$ H of external inductance resonates at 500 kHz. Left unchecked, this causes a peaking in the filter gain.

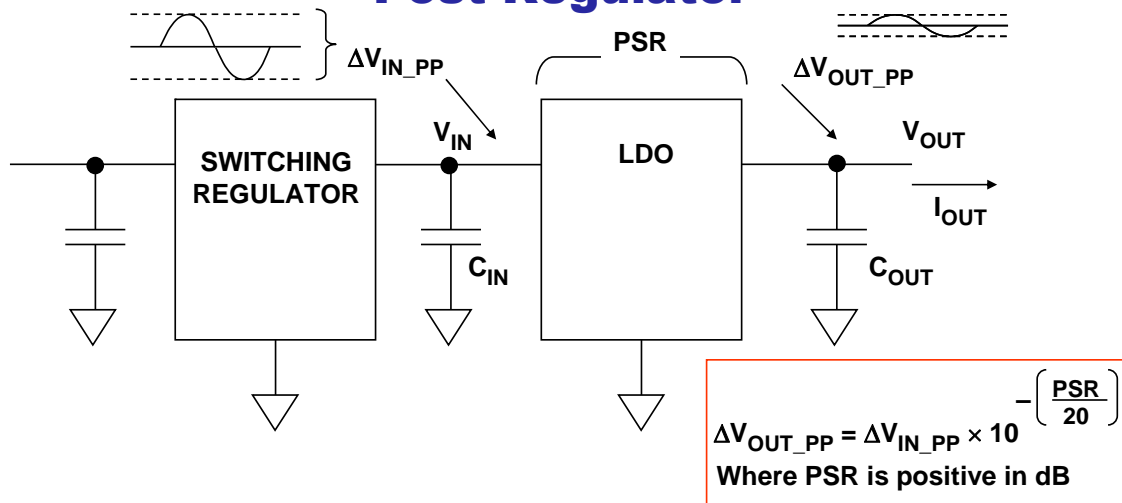
Should an undesired power line resonance be present, the effect may be minimized by lowering the Q of the inductance. This is most easily done by inserting a small resistance ( $\sim 10\ \Omega$ ) in the power line close to the IC, as shown in the right case (B).

The resistance should be kept as low as possible to minimize the voltage drop across the resistor. The resistor should be as large as needed, but no larger. An alternative to a resistor is a small ferrite bead which looks primarily resistive at the resonant frequency (see page 3.62).

# Reducing Power Supply Noise Using LDO Post Regulators

[www.analog.com/ldo](http://www.analog.com/ldo)

## Reducing Ripple Using an LDO as a Post Regulator

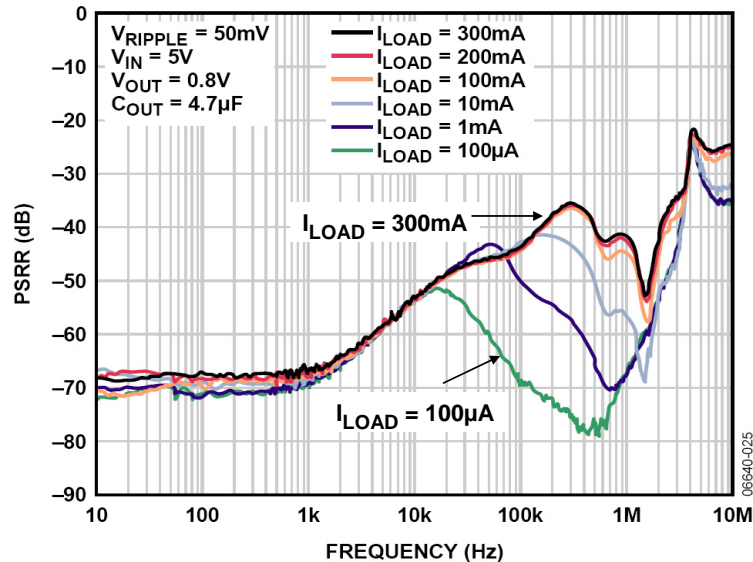


- ◆ Typical PSR @ 1MHz = 35dB to 60dB
- ◆ Specified for a given value of output capacitance,  $C_{OUT}$
- ◆ Adding additional capacitance improves PSR
- ◆ However, LDO must be stable for selected value of  $C_{OUT}$
- ◆ PSR increases for small load currents
- ◆ PSR is a function of  $V_{IN} - V_{OUT}$

It is a common misconception that LDO post regulators provide excellent filtering for power supply noise. This is certainly true at low frequencies, but the PSR of many LDOs at typical switching frequencies is surprisingly low—somewhere between about 35 dB and 60 dB at 1 MHz. This PSR is primarily determined by the internal LDO buffer amplifier.

The LDO PSR is a function of output capacitance, load current, and the difference between the input and output voltage,  $V_{IN} - V_{OUT}$ . These variables must be specified in order for the PSR to be meaningful.

## ADP1708 1A CMOS LDO PSR



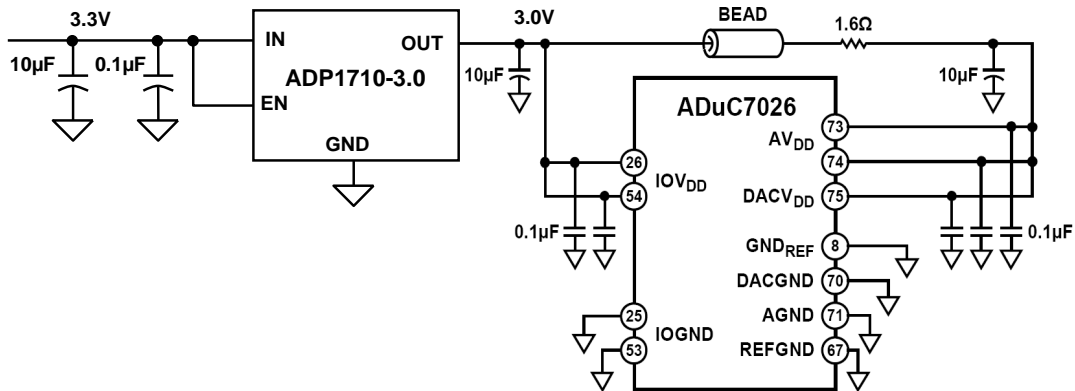
**"Dip" in curves due to output capacitance self-resonance**

This shows the PSR of the ADP1708 1 A CMOS LDO as a function of frequency and load current. The "dip" in the PSR curves is more pronounced for small load currents, and is due to the output capacitor self-resonance. In the above example, the resonant frequency of the  $4.7\mu\text{F}$  capacitor and its  $50\text{ nH}$  ESL is approximately  $300\text{ kHz}$ .

Data sheets for LDOs typically give the PSR for a number of input/output voltages. The data in this graph is for an input voltage of  $5\text{ V}$  and an output voltage of  $0.8\text{ V}$ . PSR typically decreases as  $V_{IN} - V_{OUT}$  decreases and approaches the dropout voltage.

The ADP220/ADP221 low noise, high PSRR LDO has  $60\text{ dB}$  PSR at  $100\text{ kHz}$  for an input voltage of  $3.3\text{ V}$ , an output voltage of  $2.8\text{ V}$ , and an output current of  $100\text{ mA}$ .

## Powering the ADuC7026 MicroConverter with the ADP1710 150mA LDO



In many cases it is wise to power the MicroConverter from an LDO rather than the noisy digital system supply. This figure shows the ADP1710 150 mA LDO supplying the 3.0 V to the ADuC7026 MicroConverter.

The ADP1710 supplies the  $IOV_{DD}$  digital power directly, and the  $AV_{DD}$  voltage is filtered with the ferrite bead, 1.6  $\Omega$  resistor, and 10  $\mu$ F capacitor. The 0.1  $\mu$ F capacitors are MLCC types and are placed directly at the IC power pins.

The ADP1710 has approximately 45 dB PSR at 1 MHz in the configuration shown in the figure.



## LDO Regulator Noise

- ◆ LDO noise specified in several ways, but usually the RMS noise in a bandwidth of 10Hz to 100kHz
- ◆ Noise specification must give values of input and output capacitors
  - ADP1706-series is 125 $\mu$ V rms from 10Hz to 100kHz for  $C_{IN} = C_{OUT} = 4.7\mu$ F. This corresponds to a noise spectral density of  $125\mu\text{V}/\sqrt{(100\text{kHz})} = 395\text{nV}/\sqrt{\text{Hz}}$
  - ADP220/ADP221-series has 50 $\mu$ V rms noise from 10Hz to 100kHz for  $C_{IN} = C_{OUT} = 1\mu$ F
- ◆ As with voltage references, a "noise reduction" pin may be available.
  - ADP1710 noise = 330 $\mu$ V rms from 10Hz to 100kHz,  $C_{IN} = C_{OUT} = 1\mu$ F, no noise reduction pin.
  - ADP1711 noise = 40 $\mu$ V rms from 10Hz to 100kHz with 10nF capacitor on noise reduction pin.

LDO noise can be specified in a number of ways. Regardless of the method, it must be specified for given values of input and output capacitors.

In most cases, LDO noise is specified as an rms voltage over a 10 Hz to 100 kHz bandwidth.

The equivalent noise spectral density can be calculated by dividing this rms voltage by the square root of the measurement bandwidth. For the ADP1706 series, the rms noise in the 100 kHz bandwidth is 125  $\mu$ V rms, corresponding to a noise spectral density of approximately 395 nV/ $\sqrt{\text{Hz}}$ .

For the ADP220/ADP221, the noise is 50  $\mu$ V rms from 10 Hz to 100 kHz with an input voltage of 3.3 V, an output voltage of 2.8 V, and an output current of 100 mA.

In some cases, a "noise reduction" pin may be available, as in the case of the ADP1711. Bypassing this pin with a 10 nF capacitor can reduce the rms noise from 125  $\mu$ V to 40  $\mu$ V rms.

Further LC filtering on the LDO output can reduce the noise even further if system requirements dictate.

## **Reducing Power Supply Noise by Physical Separation from Analog Circuits**

## Types of Coupling

- ◆ **Conducted (Most focus on this)**
  - **Noise on Power Supplies**
  - **Remedies**
    - ◆ **Low Impedance Ground Planes**
    - ◆ **Filtering and Decoupling**
    - ◆ **Component Layout**
- ◆ **Radiated (This is important also)**
  - **Primarily from Magnetic Switching Regulators**
  - **Remedies**
    - ◆ **Physical Separation from Analog Circuits**
    - ◆ **Component Layout (Minimize Loops)**
    - ◆ **Shielded Magnetic Devices**
    - ◆ **Add Extra Shielding**
- ◆ **PHYSICAL SEPARATION AVOIDS NOISE!**

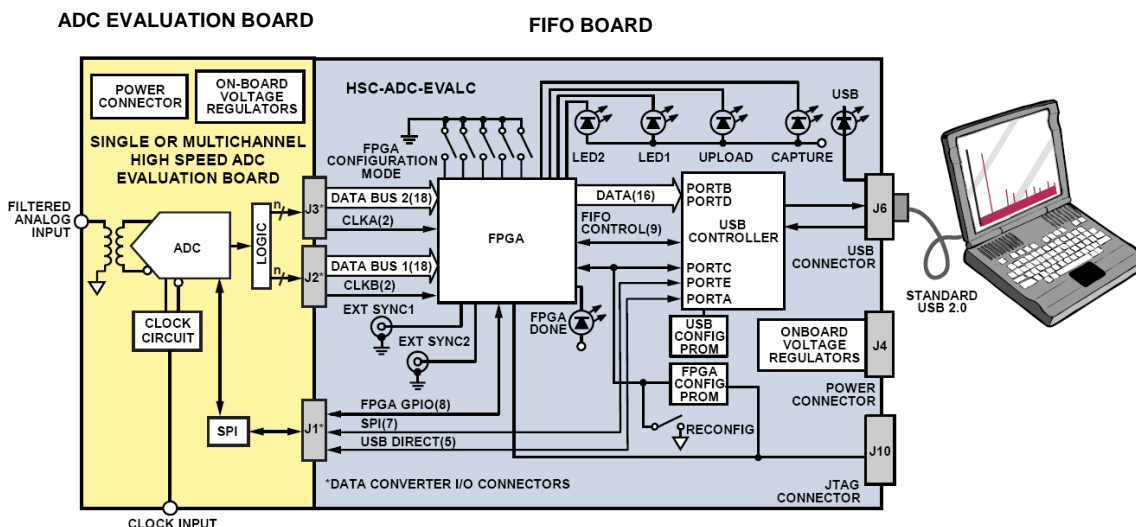
Quite a bit of attention is given to conducted noise on power supplies, ground planes, etc. Most designers address these problems with the use of filtering and decoupling techniques.

Another often neglected source of noise is that due to radiation, primarily from magnetic elements such as the inductors used in switching regulators. The high  $dv/dt$  and  $di/dt$  in these circuits often couples into the ground plane and any nearby circuits.

A very effective (and often overlooked) technique for reducing the effect of this type of noise is to simply separate sensitive circuits from the noisy ones. The magnetic field coupling decreases with the square of the distance of separation.

Proper component layout, physical separation, and the addition of extra shielding if required can usually eliminate most noise coupling problems.

# ADC/FPGA System Evaluation Board Power Design (Physical Separation Avoids Noise)



The Analog Devices' high speed ADC evaluation board system is a good example of proper component layout and signal routing. It encompasses several functions commonly found in modern systems:

- High speed, high performance ADC (12 to 16 bits, up to 250 MSPS)
- Clock generation circuits
- High speed FPGA for buffering ADC output data (Xilinx Virtex-4)
- USB and FPGA configuration EPROMs
- Control functions for interfaces and USB
- Point-of-load regulators for supply voltages

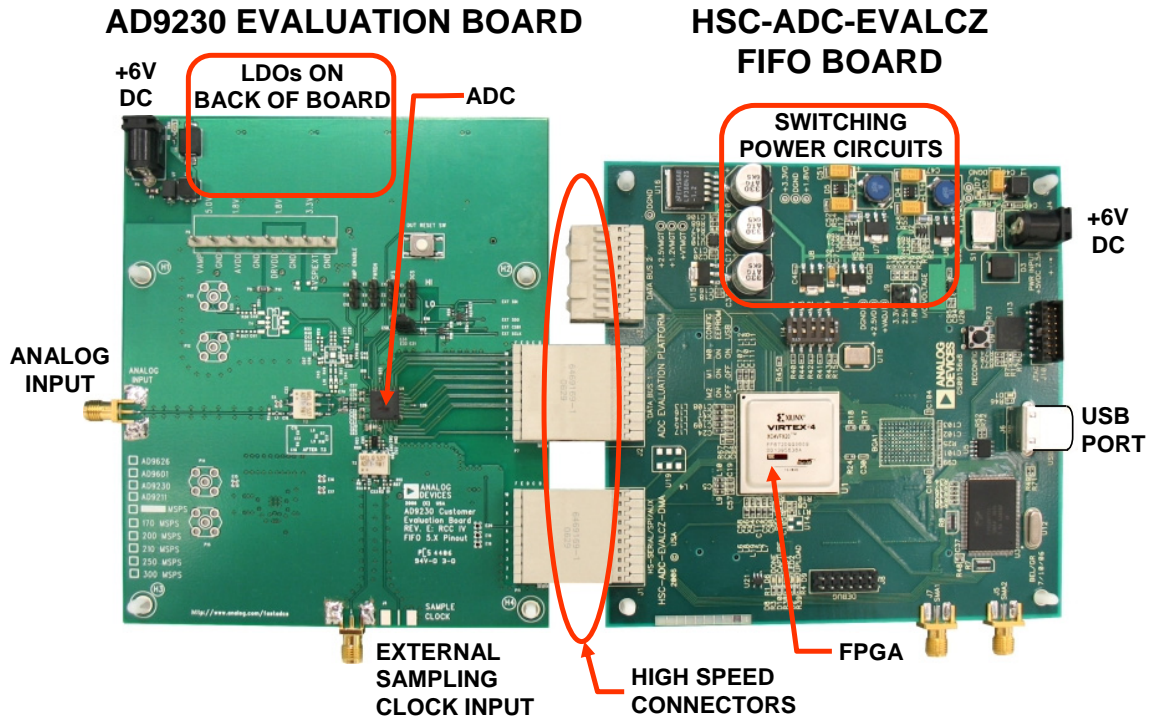
The system is designed to use a common memory board which interfaces to product-specific ADC evaluation boards. Connection between the two boards is made using high speed connectors.

Because this system is used to evaluate ADCs with high SFDR (>90 dB) and SNR (>80 dB) its layout has been optimized to achieve the maximum performance possible.

The boards have 4-layers with two outer components and signal layers, a ground plane layer, and a power plane layer. The boards use a single ground plane, but analog components are separated from digital components.

Switching supplies are used to power the FIFO board, and LDOs power the ADC on the evaluation board.

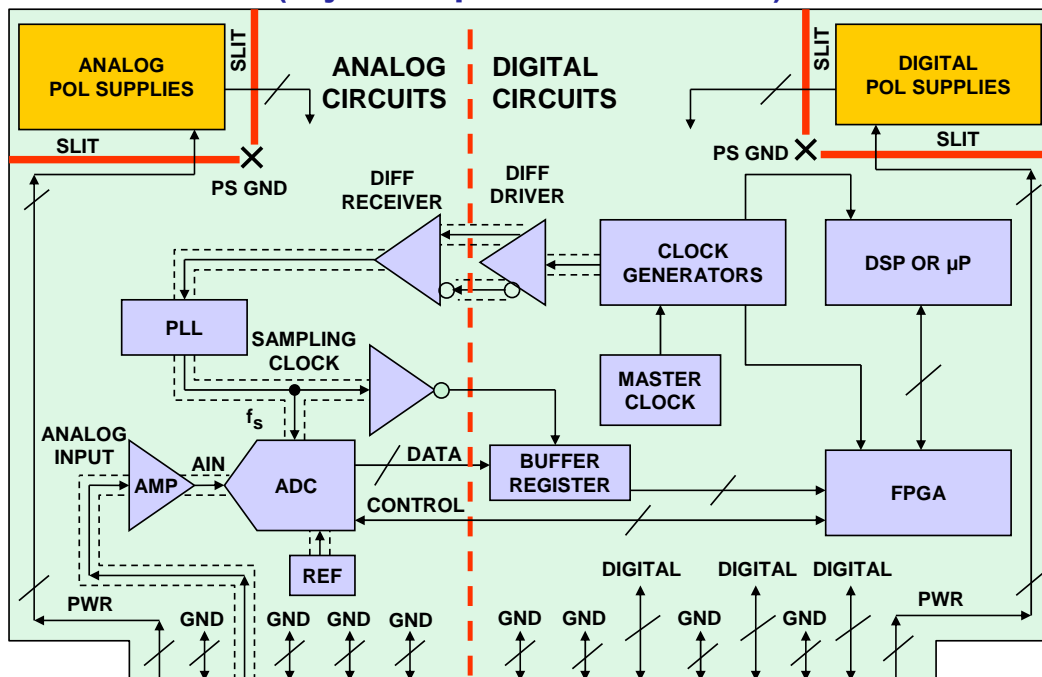
## ADC/FPGA System Board Layouts (Physical Separation Avoids Noise)



This shows a photo of an actual ADC evaluation board connected to the FIFO board. Note the location of the power circuits on each board.

The CAD files are available for all Analog Devices' evaluation boards and can be helpful in system layout.

## Optimum PCB Layout Begins with Critical Component Placement (Physical Separation Avoids Noise)



This is an optimum PC board layout which incorporates many components in a typical system.

The dotted PCB traces are extremely critical and are kept well away from any digital traces. Note that the PLL which generates the sampling clock is located on the analog side of the board close to the ADC.

The digital circuits are located on the right side of the board. The master clock is transmitted across the interface using a differential driver and receiver and then to the PLL. The function of the PLL is to "clean up" the noisy digital clock and reduce phase noise and jitter.

The analog and digital POL supplies are located away from the rest of the circuits. This is especially important if switching converters are used. The ground plane is slit so that the noisy switching currents are isolated from the ground plane. This corresponds to the "power ground" point in the switching supply circuit.

At least 30% of the connector pins should be dedicated to ground. Ground pins are used to isolate the critical analog input signal from the other traces. Ground and power can be used to isolate other signals as well.

## **Noise and Ripple Reduction Techniques Summary**

- ◆ Proper Layout and Grounding (using Ground Plane) Mandatory
- ◆ Low ESL/ESR Capacitors Give Best Results
- ◆ External LC Filters Very Effective in Reducing Ripple
- ◆ Use simulated LC filter initially, then prototype
- ◆ Completely Analytical Approach Difficult, Prototyping is Required for Optimum Results
- ◆ Linear Post Regulation Effective for Noise Reduction and Best Regulation
- ◆ High Frequency Localized Decoupling at IC Power Pins is Still Required
- ◆ Once Design is Finalized, Do Not Switch Vendors or Use Parts Substitutions Without First Verifying Their Performance in Circuit
- ◆ PHYSICAL SEPARATION AVOIDS NOISE

This summarizes noise and ripple techniques discussed thus far in this section. Section 4 discusses layout issues related to switching regulators.

## **Reducing Noise in Mixed-Signal Circuits by Proper Grounding**

Before starting this somewhat controversial topic, we should make it clear that there is no single foolproof method for system grounding. What we can do is point out some general principles that are correct and let you apply them to your own system design.

One concept that is not subject to interpretation is that at least one low impedance ground plane is required in practically all systems. In addition, power supplies must be properly decoupled to the ground plane as previously discussed.

In some systems, two ground planes are used: an analog ground plane for sensitive analog circuits, and a digital ground plane for noisy digital circuits. Each printed circuit board has two such non-overlapping ground planes, and they are kept separate until they are ultimately joined at one point which becomes the system "star" ground point.

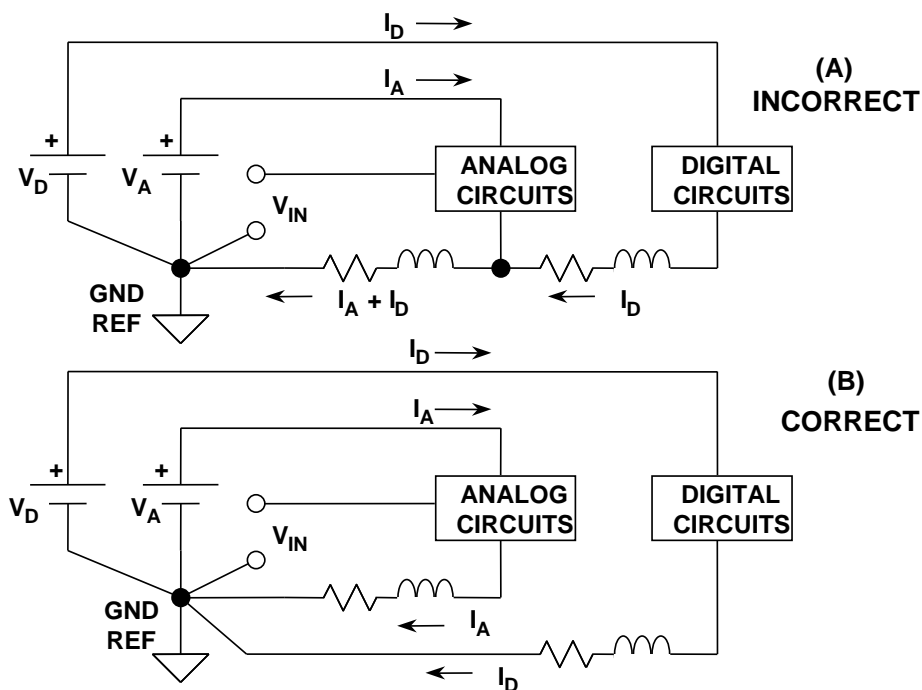
In some systems, a single ground plane for both analog and digital circuits is used, and the desired system performance is also achieved.

Some customers start out using the split ground approach and later find that the single ground plane gives better performance.

In this section we will illustrate both approaches and focus on how mixed-signal components should be grounded—an issue which seems to confound many engineers.



## Digital Currents Flowing in Analog Return Path Create Error Voltages



Because ground is the power return for all digital circuits, as well as many analog circuits, one of the most basic design philosophies is to separate digital ground returns from analog ground returns.

If the ground returns are not separated, not only does the return current from the analog circuitry flow through the analog ground impedance, but the digital ground current also flows through the analog ground return, and the noisy digital ground current is typically much greater than the analog ground current. This produces unwanted noise at the  $V_{IN}$  input to the analog circuit as shown in (A). Remember, grounds are not zero impedance.

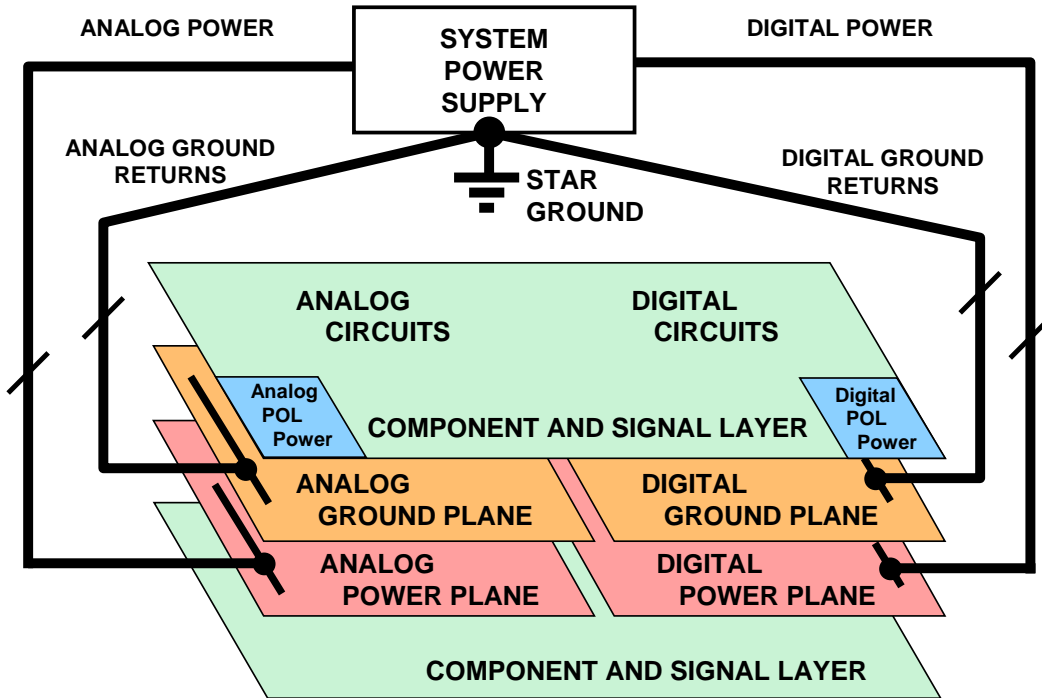
As the frequency of digital circuits increases, the noise generated on the ground increases dramatically. TTL and CMOS logic families are of the saturating types. This means that the logic transitions cause large transient currents on the power supply and ground. CMOS outputs basically connect the power to ground through a low impedance during the logic transitions.

And it's not just the basic clock rate that is a problem. Digital logic waveforms are basically rectangular waves, which implies many higher frequency harmonic components, starting at the fundamental clock rate.

The preferred method is shown in the lower diagram (B) where the analog and digital current return paths are separate and are joined at a single ground reference point.

While this concept is relatively easy to illustrate in a diagram, implementing it in an actual system can be quite complex because of the many return paths required. This is where the ground plane comes to the rescue (sometimes).

## Simple Four Layer Board Stack with Split Analog and Digital Ground Planes



A key concept in grounding is that both the power and ground return paths should have the lowest impedance possible, i.e., the parasitic inductance and resistance should be kept to a minimum. In a practical system this is accomplished by the use of PC boards with ground and power planes.

A simple two-layer board needs one layer for ground and the other layer for signal and power runs. For dense boards with lots of interconnections, it is difficult to maintain a reasonably solid ground plane because of signal and power crossovers. For this reason, modern systems generally use multilayer PC boards.

This figure shows a simple four-layer multilayer board stack which incorporates the principles of analog/digital ground return separation shown in the previous diagram. The outer two layers are for signal traces and components, and the inner two are for power and ground. Most of the ICs are generally mounted on one of the outer layers, and the other outer layer reserved for signals and perhaps decoupling capacitors and inductors.

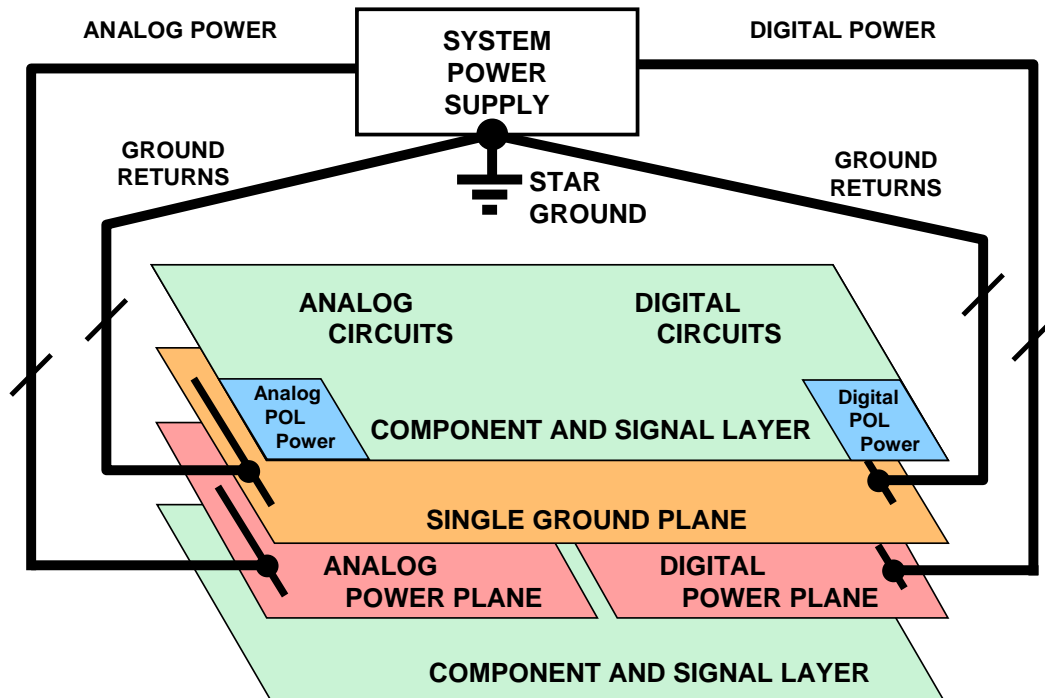
The analog components are grounded to the analog ground plane, and the digital components to the digital ground plane.

Note that the analog ground plane is kept separate from the digital ground plane all the way back to the main system power supply. In addition, there will be point-of-load regulators on the PC board where required. The analog and digital power supplies are also kept separate.

The analog ground plane should not overlap the digital ground plane because the inter-plane capacitance will cause unwanted noise coupling. The capacitance of a trace over a ground plane is approximately 2.8 pF/cm<sup>2</sup> for a standard PC board.

In a multiboard system the power and ground connections to the PC board are made through a connector which is usually located on one edge of the board, unlike the diagram above.

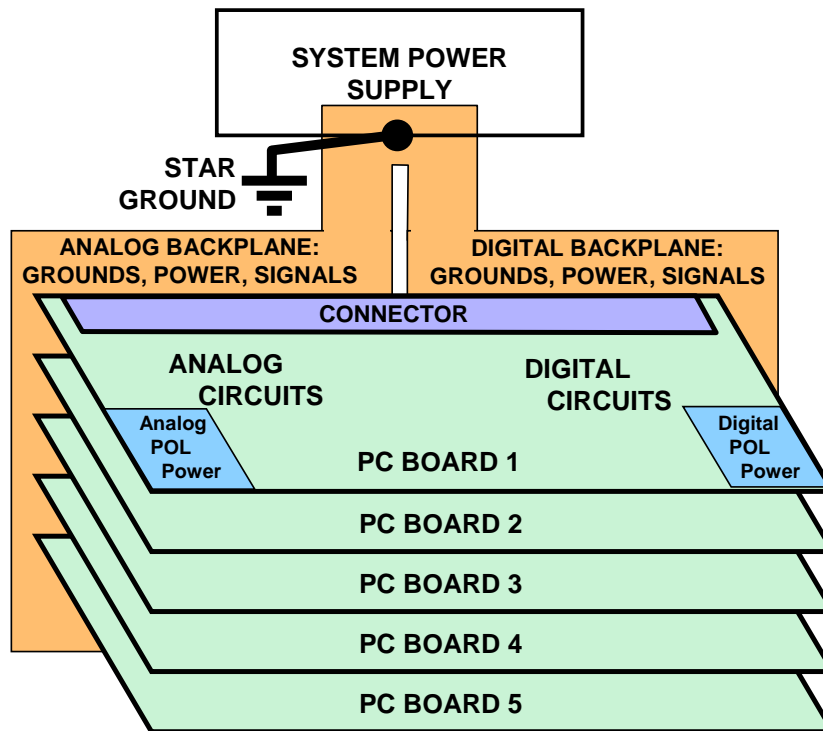
## Simple Four Layer Board Stack with Single Ground Plane



Some systems can be designed using a single ground plane for both analog and digital components. This is especially true if the digital circuits are minimal and have relatively low  $dv/dt$  outputs.

This four layer PC board utilizes a single ground plane for both analog and digital circuits, but the analog circuits are still physically separated from the digital ones.

## Maintaining Low Impedance to Power Supply



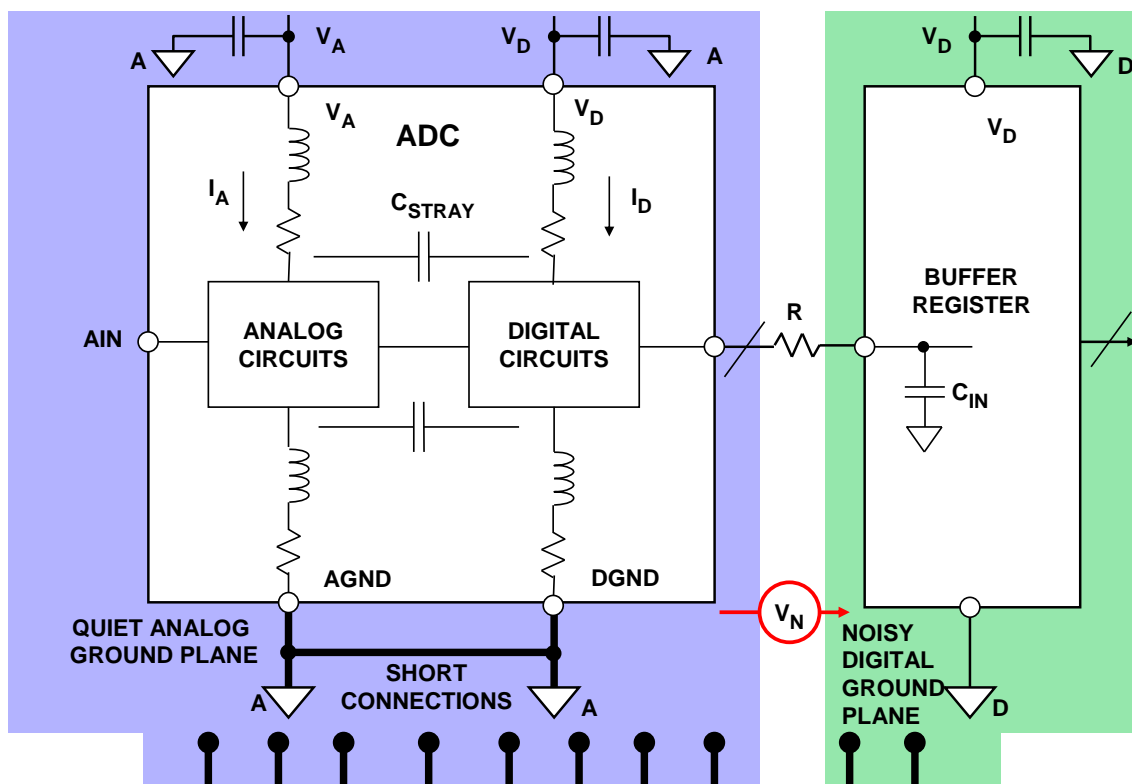
The previous figure showed a single PC board, but most systems require multiple boards as shown here. This shows how the low impedance PC board ground is carried through multiple pins on the connectors to the backplane ground planes and then to the system power supply.

If the system is using split analog and digital ground planes, then they should remain separated on the backplane and joined at the system power supply.

If the system uses a single ground plane, then the PC board ground planes are connected to the backplane ground plane without separation.



## Split Ground Planes, Connected at System PS



In a system with split ground planes, the AGND and DGND pins should be connected to each other and to the analog ground plane with short connections as shown here. The digital currents generated by the ADC are typically fairly low and can be isolated by proper decoupling of the ADC  $V_D$  power pin.

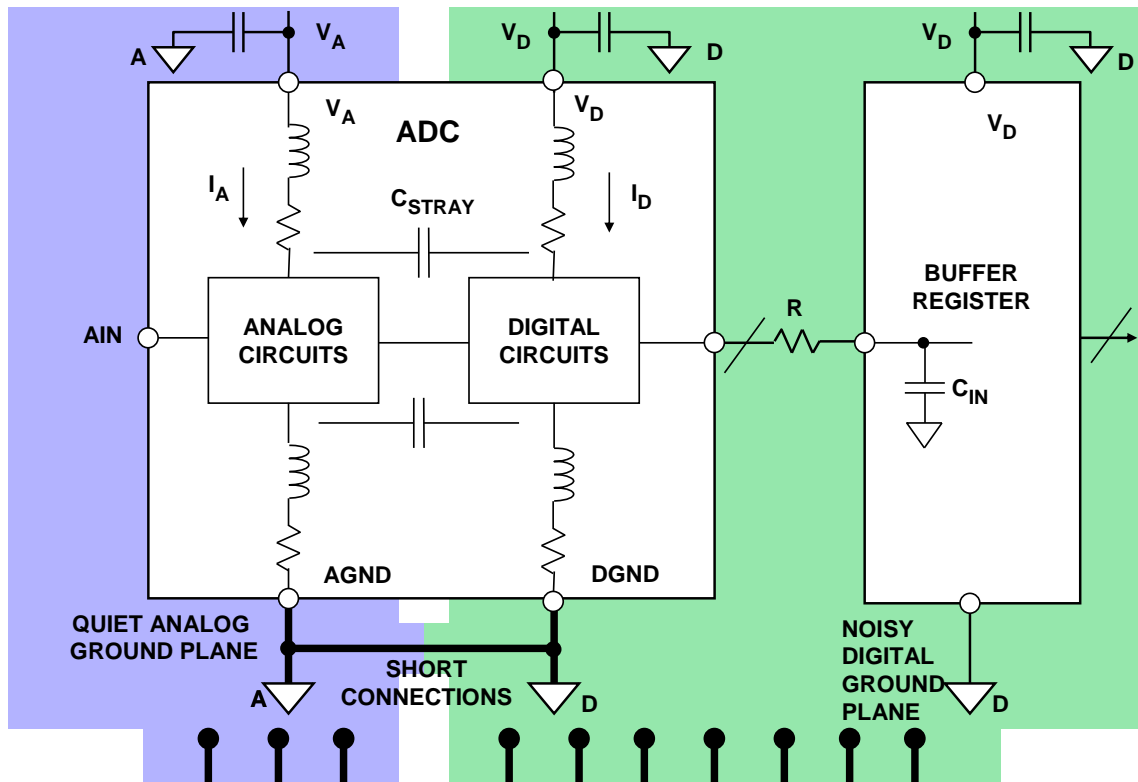
The noise between the two planes appears at the digital interface where it results in a slight degradation in noise margin. If the digital outputs of the ADC are differential (LVDS, PECL, or CML, for example) then the noise between the two planes will be common-mode and mostly rejected by the differential receiver.

The digital outputs of the ADC have fast edges, so a small resistor ( $50\ \Omega$  to  $500\ \Omega$ ) should be inserted to isolate the high  $dv/dt$  digital outputs from the input capacitance of the buffer register. The digital outputs should have minimum fan out in order to minimize digital currents due to capacitive loading. Under no circumstances should the digital outputs of a high performance converter be connected to a noisy data bus. An intermediate buffer register should always be used as shown here.

The series resistor value should be chosen so that the RC time constant is less than about  $0.1T$ , where  $T$  is the period of the data rate frequency on the output pin. This is to ensure that the data settling time is not significantly degraded by the additional time constant.

It should be noted that the loop area formed by returning the currents to the power supply must also be considered, especially at high frequencies.

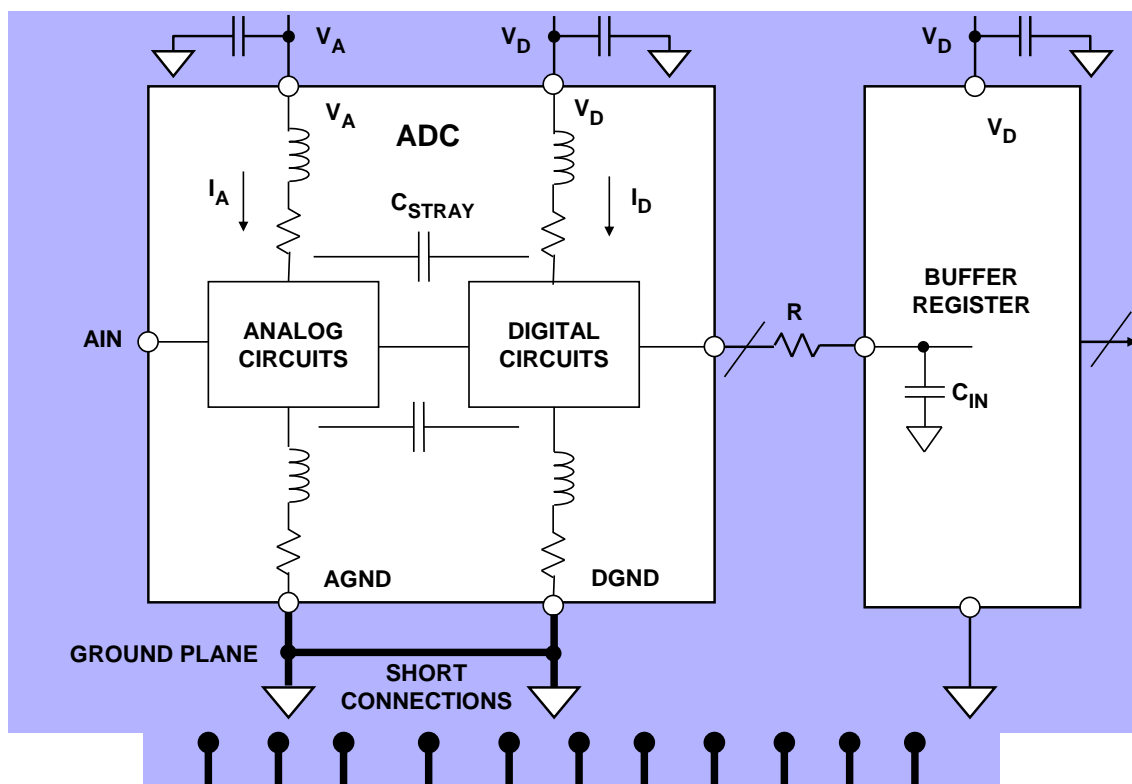
## Split Ground Planes, Connected at ADC



In a system with a single PC board, the analog and digital ground planes can be separated as shown but must be joined together at the ADC with very short connections. This layout is often seen on ADC evaluation boards and is an effective way of separating analog and digital currents.

In systems with multiple ADCs and PC boards, this approach creates a connection between the analog and digital ground planes at each ADC. These multiple connections may create unwanted ground loops.

## Single Ground Plane



In some systems, a single ground plane can be used provided the analog and digital circuits are physically isolated. As before, the  $AGND$  and  $DGND$  pins should be connected to each other and to the ground plane with short connections.

The choice between split and single ground planes is not an easy one to make. The conservative approach is to initially design the PC boards with split ground planes but provide extra vias which can later be used to "jumper" the planes together. Performance can be measured under both conditions.

As a general rule, systems with lots of high current digital circuitry are more likely to benefit from the split ground approach than systems with moderate digital currents.



## Technical References

## Analog Devices' Textbook References

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. See Chapter 12.
2. Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410. See Chapter 9.
3. Walt Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN: 0-916550-26-5. Also available as *Op Amp Applications Handbook*, Elsevier-Newnes, 2004, ISBN: 0-7506-7844-5. See Chapter 7.

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3. Howard W. Johnson and Martin Graham, *High-Speed Digital Design*, PTR Prentice Hall, 1993, ISBN: 0133957241.
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5. Ralph Morrison, *Solving Interference Problems in Electronics*, John Wiley, 1995.
6. C. D. Motchenbacher and J. A. Connelly, *Low Noise Electronic System Design*, John Wiley, 1993.
7. Mark Montrose, *EMC and the Printed Circuit Board*, IEEE Press, 1999 (IEEE Order Number PC5756).
8. Eric Bogatin, *Signal Integrity–Simplified*, Prentice Hall, 2003, ISBN-10: 0130669466, ISBN-13: 978-0130669469.
9. Stephen H. Hall, *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*, Wiley-IEEE Press, 2000, ISBN-10: 0471360902, ISBN-13: 978-0471360902.

## Notes:

## Practical Power Solutions

1. Point-of-Load Power
2. System Power Management and Portable Power
3. Power for Mixed Analog/Digital Systems
4. Hardware Design Techniques

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### SECTION 4 HARDWARE DESIGN TECHNIQUES

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Active Components.....	4.39
Power Supply Layout and Grounding.....	4.52
Shielding.....	4.73
Thermal Design.....	4.76
Technical References.....	4.84

# Passive Components

Passive components play a significant role in the operation of switch mode power supplies (SMPS). Inductors are the primary energy storage device in most SMPS. Capacitors are used for filtering, decoupling, energy storage, and affect the design of the compensation network since the SMPS is a closed-loop feedback system. Resistor dividers are often used to set the output voltage, and low value resistors are often used in current sense applications.

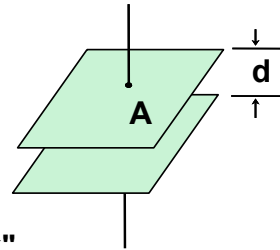
# Capacitors



- ◆ A capacitor is an energy storage element constructed of 2 conductors separated by an insulating material

$$C = \epsilon \cdot \epsilon_0 \cdot \frac{A}{d}$$

$$E_{\text{STORED}} = \frac{1}{2} \cdot C \cdot V^2$$



- ◆ Where
  - $\epsilon_0$  is the dielectric constant of free space
  - $\epsilon$  is the relative dielectric constant of insulator
  - $\epsilon$  is sometimes called the "k-factor" or simply "k"
  - A is area of conductive plates
  - d is distance between plates
  - V is the voltage potential across plates
- ◆ Larger capacitors have larger capacitance, and therefore better energy storage.
- ◆ Different capacitors use different dielectric material. This changes capacitance and their characteristics (ESR, Current Rating, DC Bias, etc) in power designs

This figure shows the basics of capacitors.

Capacitors come in a wide variety of sizes, both in capacitance value and physical size. Choosing the right capacitor for a specific application can be crucial to the proper operation of the circuit. Choosing the right capacitor means not only choosing the correct value but also the right dielectric material as well. As we will see in the following pages, real world capacitors are far from ideal, especially over a wide frequency range.

The capacitance can be calculated from the information in this figure. It is dependant on the dimensions of parallel conductors, the separation of the conductors, and the dielectric constant of the insulator. The capacitive impedance can be calculated from:

$$Z_C = 1/j\omega C$$

where:

$$j = \sqrt{-1}$$

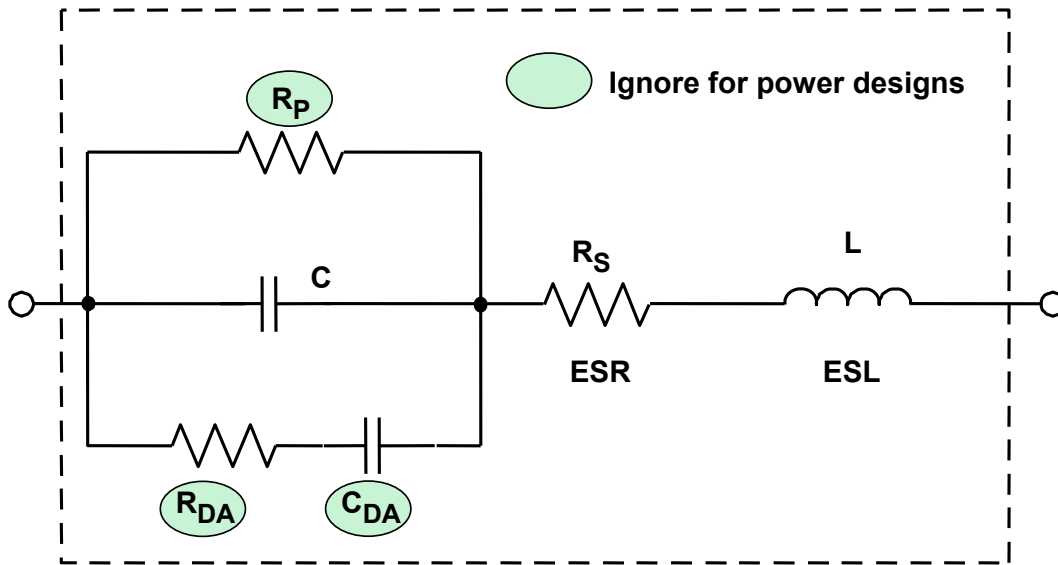
and

$$\omega = \text{radian frequency} = 2\pi \cdot \text{frequency in Hertz.}$$

The energy stored in the capacitor which is charged to a voltage, V, is given by the formula:

$$E = 0.5CV^2$$

## A Real Capacitor Equivalent Circuit Includes Parasitic Elements



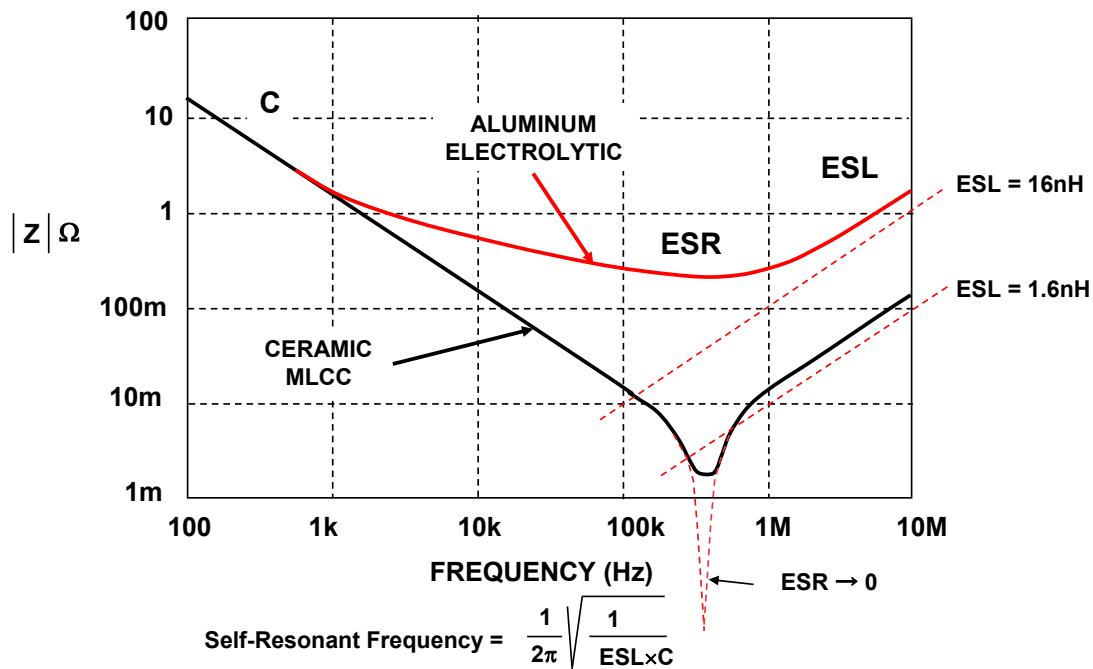
This is a workable model of a non-ideal capacitor. The nominal capacitance,  $C$ , is shunted by a resistance,  $R_p$ , which represents insulation resistance or leakage. A second resistance,  $R_s$ , (equivalent series resistance, or ESR), appears in series with the capacitor and represents the resistance of the capacitor leads and plates.

Note that elements in the capacitor equivalent circuit aren't that easy to separate. The model is for convenience in explanation. Inductance,  $L$  (equivalent series inductance, or ESL), models the inductance of the leads and plates. Finally, resistance  $R_{DA}$  and capacitance  $C_{DA}$  together form a simplified model of a phenomenon known as *dielectric absorption*, or DA. This can degrade fast and slow circuit dynamic performance. In a real capacitor,  $R_{DA}$  and  $C_{DA}$  may actually consist of multiple parallel sets.

In most cases the values of  $R_p$ ,  $R_{DA}$ , and  $C_{DA}$  are more important in high frequency (RF) applications. We will neglect them in most power supply applications and focus on  $C$ ,  $ESR$ , and  $ESL$ .



## "Bathtub" Impedance of 100μF Capacitors



Theory tells us that the impedance of a capacitor will decrease monotonically as frequency is increased. Practice tells us that at some frequency the ESR will dominate, and the impedance plot will flatten out. In fact, as we continue up in frequency, the impedance will start to rise. This is where the ESL starts to dominate. Where these "knee" points occur will vary with capacitor construction, dielectric, and value.

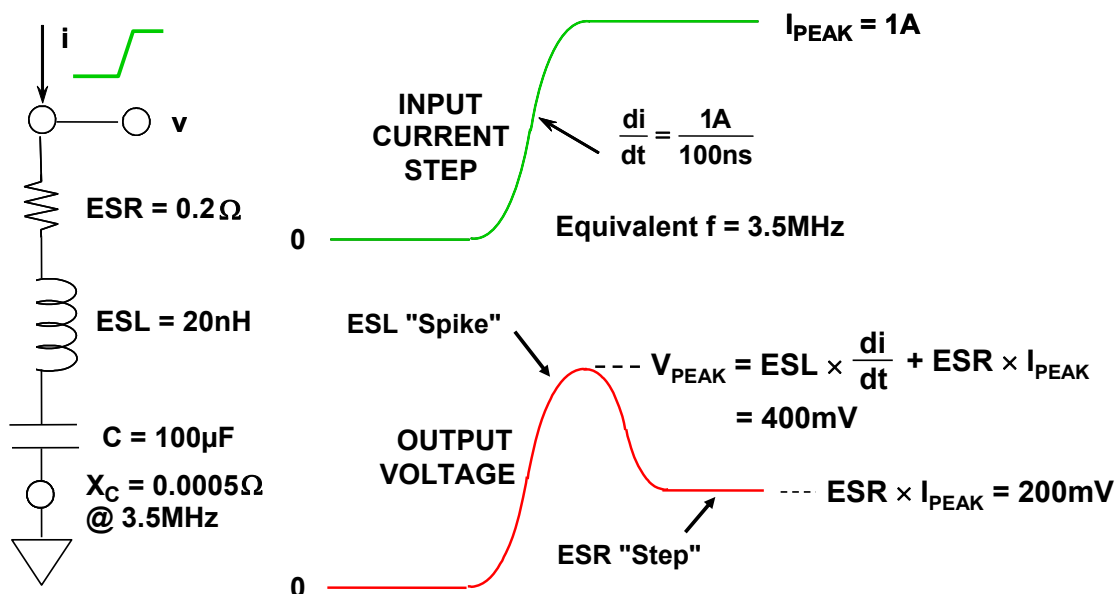
This is why we often see larger value capacitors paralleled with smaller values. The smaller value capacitor will typically have lower ESL and continue to "look" like a capacitor higher in frequency. This improves the overall performance of the parallel combination over a wider frequency range.

The self-resonant frequency of the capacitor is the frequency at which the reactance of the capacitor,  $1/\omega C$ , is equal to the reactance of the ESL,  $\omega \times \text{ESL}$ .

This figure compares the impedance of a 100 μF aluminum electrolytic capacitor with a 100 μF multi-layer ceramic capacitor (MLCC). Note that the ceramic capacitor has a much lower ESL and ESR than the aluminum electrolytic. Therefore the "dip" at the ceramic capacitor's self resonant frequency is much more pronounced than the dip in the aluminum electrolytic.

An ideal capacitor with  $\text{ESR} = 0$  has an infinite "dip" at the self-resonant frequency as shown in the figure.

## Response of a Capacitor to a Current Step



The complex impedance of a “real” capacitor will also cause non-ideal response to a current step. The assumption here is that we are stepping from a steady state current of 0 A to a steady state of 1 A. We also assume that the rise time of the current step is about 100 ns, which corresponds to a frequency of about 3.5 MHz. A “perfect” 100  $\mu\text{F}$  capacitor has an impedance of 0.5 m $\Omega$  at 3.5 MHz.

We would expect to see the capacitor voltage start at zero (the voltage across an ideal capacitor cannot change instantaneously) and then slew at a rate equal to  $I_{PEAK}/C$  (which in this case works out to be 10,000 V/s, or 10 mV/ $\mu\text{s}$ ). The ideal capacitor should have only a small voltage change during the 100 ns rise time of the current step. (Approximately  $1 \text{ A} \times 0.0005 \Omega = 500 \mu\text{V}$ ).

The actual response of the non-ideal capacitor ( $ESR = 0.2 \Omega$ ,  $ESL = 20 \mu\text{H}$ ) is shown in the figure.

The fast-rising edge of the current waveform shown results in an initial voltage peak across the capacitor, which is proportional to the ESL. The current through the inductor cannot change instantaneously. After the initial inductive transient, the voltage settles down to a longer duration level which is proportional to the ESR of the capacitor. Thus the ESL determines how effective a filter the capacitor is for the fastest components of the current signal, and the ESR is important for longer time frame components.

Note that an overall time frame of a few microseconds (or even less) is relevant here. As things turn out, this means switching frequencies in the 100 kHz to 1 MHz range. Unfortunately this happens to be the region where many switching supplies operate, and the ESR and ESL effects become critical.

## Capacitor Data Sheet : What Do Specs Mean ?

Size code	SANYO Part number	Rated Voltage (V)	Rated Temperature (°C)	Rated Capacitance (μF)	D.F. (%max.)	L.C. (μA) max./5min.	E.S.R. (mΩmax.) 100kHz/20°C	Maximum allowable ripple current (mA <sub>rms</sub> ) 100kHz <sup>ripple</sup>
	10TPB47M	10.0	105	47	8.0	47.0	70	1100
	10TPB33M	10.0	105	33	8.0	33.0	70	1100

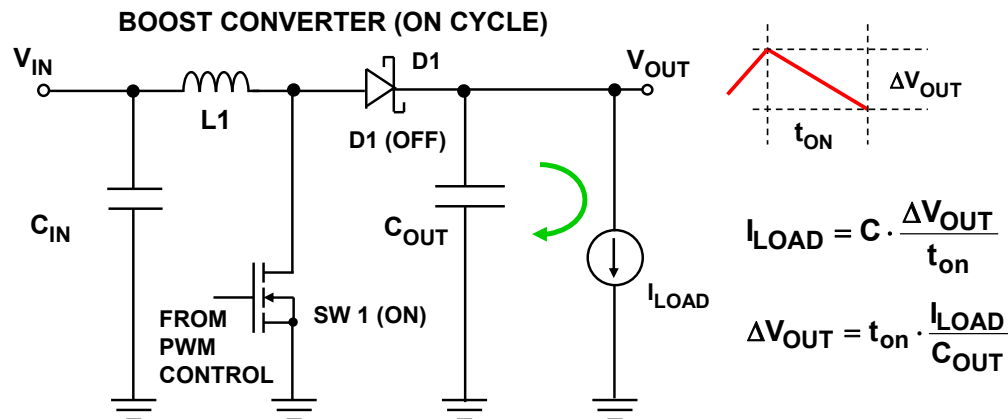
- ◆ **Rated Voltage:** Maximum voltage for which the capacitor is guaranteed to function. Often there is no guarantee of actual capacitance at this voltage.
- ◆ **Rated Temperature:** Maximum operating temperature. Temperature rise of capacitor based on ripple current should be included.
- ◆ **Rated Capacitance:** Usually specified to  $\pm 20\%$  or  $\pm 30\%$ . Note this is the capacitance at no dc bias and at low frequency. Always look at data sheet plots to check predicted capacitance at your design conditions (especially dc bias).
- ◆ **Dissipation Factor, DF:** This is a measure of the power loss of the capacitor expressed as a %.  $DF = 2\pi fRC \times 100\%$ , where  $R = ESR$ ,  $f =$  frequency (Hz)
- ◆ **Leakage Current, LC:** The amount of leakage current after a specified amount of continuous operation (5 to 10 minutes). Leakage current will cause the capacitor to discharge itself with no load attached.
- ◆ **Equivalent Series Resistance, ESR:** Includes conductor resistance, dielectric loss, and leakage. This is a very important specification, as it will affect load transient, ripple voltage at input and output, and maximum current capability.
- ◆ **Maximum Ripple Current:** The maximum allowed RMS current in a dc-to-dc converter application. The frequency is usually specified at 100kHz.

This figure defines the terms that you may find in a specification page for a capacitor.

Different value ranges of capacitors may have different specifications—the one shown is for a large value electrolytic. Small value capacitors may emphasize different specifications. Also you may find that capacitors targeted at different frequency applications may have ESR, etc., specified at frequencies other than 100 kHz.

We will now examine the functions of capacitors in switch mode power supplies.

## Capacitors for Power Designs: Energy Storage



- ◆ Energy stored in a capacitor increases as voltage is applied across it.
- ◆ It can provide energy quickly as required—acts as an energy reservoir.
- ◆ If load changes, capacitor will supply energy until loop can react. Larger capacitor will give better regulation.
- ◆ Larger output capacitor = less voltage ripple, neglecting ESR effects

This figure shows how the  $C_{\text{OUT}}$  output capacitor acts as an energy storage device in a boost converter.

During the time SW1 is on and D1 is off,  $C_{\text{OUT}}$  must supply all of the current to the load. The voltage will "droop" at a rate equal to  $I_{\text{LOAD}}/C_{\text{OUT}}$  until the next charge cycle (SW1 off, D1 on) replenishes this charge.

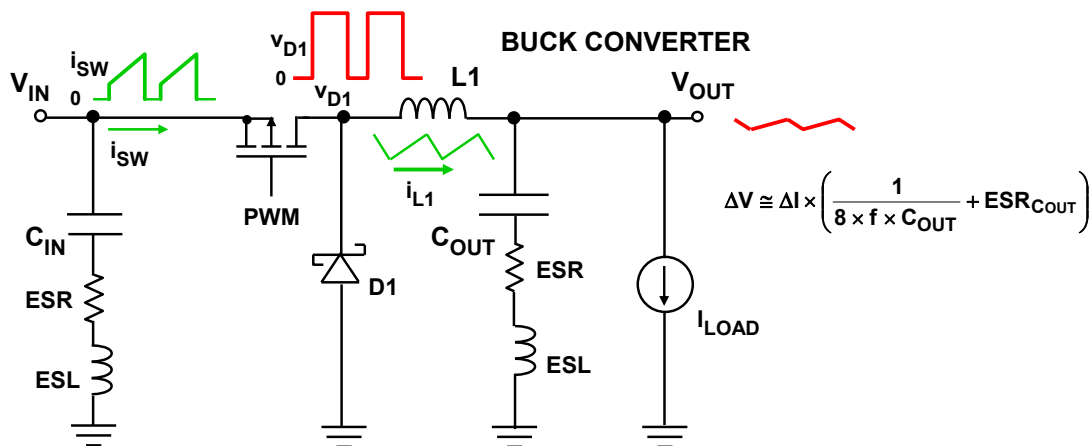
The choice of the value for  $C_{\text{OUT}}$  is a tradeoff—trying to balance capacitor (physical size), cost, and ripple current.

Since the output ripple of a boost converter current is high,  $C_{\text{OUT}}$  needs to be rated to handle the required ripple current. This generally means that the ESR will be low.

A good starting point for  $C_{\text{OUT}}$  size is to use the next standard value up from the value calculated from:

$$C_{\text{OUT}} = t_{\text{ON}} \frac{I_{\text{LOAD}}}{\Delta V_{\text{OUT}}}$$

## Capacitors for Power Designs: Filtering



- ◆ The LC filter at the output of the buck converter filters the square wave at the switch node,  $v_{D1}$ .
- ◆ The amount of voltage ripple seen at  $V_{OUT}$  is inversely proportional to the capacitor value and proportional to ESR.
- ◆ We can make C very large, so the ultimate limit is the ESR.
- ◆ The input filter capacitor will reduce the noise injected onto the  $V_{IN}$  line which can interfere with other parts of the system.

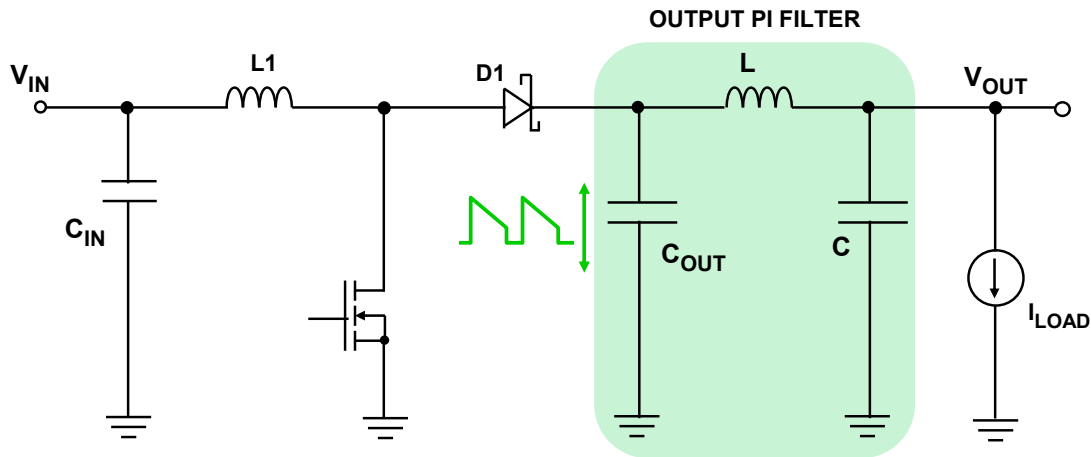
The second function of capacitors in switch mode power supplies is filtering. This shows how the  $C_{OUT}$  capacitor in a buck converter is used to reduce the output ripple voltage.

In this instance the inductor will smooth out the ripple, since the current in an inductor can't change instantaneously. While that may seem like a good thing, it should be remembered that low ripple and good transient response are mutually opposed to each other. Also the regulator is a closed loop negative feedback system, so the laws governing stability must be obeyed. The Bode plot of the system needs to be examined for adequate phase margin.

The input current of a buck converter is discontinuous, therefore the input filter capacitors must reduce the noise injected onto the  $V_{IN}$  line which can interfere with other parts of the system. The peak source impedance should be about three times lower than  $V_{IN}/I_{IN}$ .

This is generally achieved by keeping the input capacitor ESL small and  $C_{IN}$  large. Sometimes the  $C_{IN}$  ESR has to be decreased to lower the input impedance, or two capacitors in parallel are used for  $C_{IN}$ —one with small capacitance and low ESR/ESL and one with large capacitance and higher ESR/ESL.

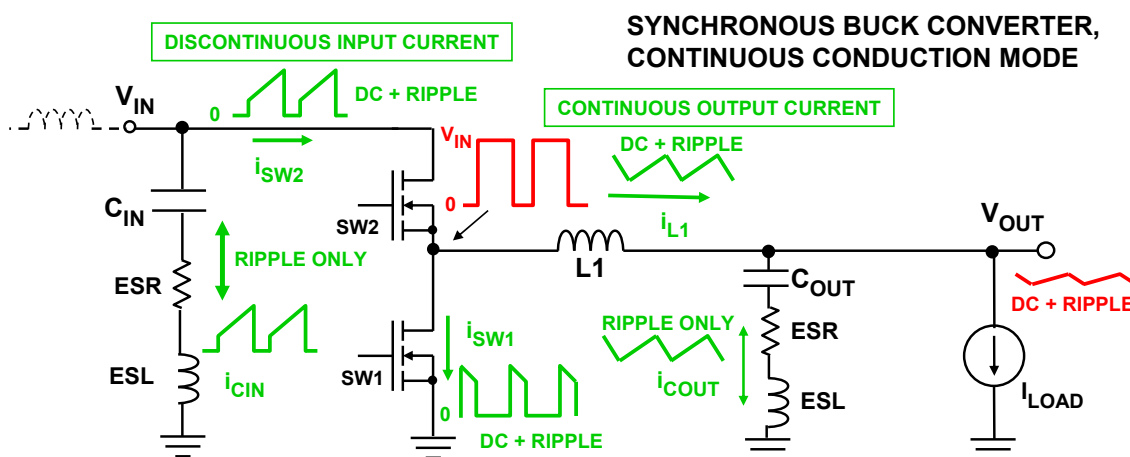
## Boost Converter with Output Pi Filter



The boost converter has a discontinuous pulsed output current which is more difficult to filter than the buck converter output. Rather than try and reduce the ripple with a single output capacitor  $C_{OUT}$ , it is often more efficient to use an output pi filter as shown in shaded area of the figure. The output noise filter inductor,  $L$ , reduces output ripple voltage by attenuating the ac current passing through the output noise filter capacitor,  $C$ . The output inductor,  $L$ , is subjected to low ac voltage and very low ac current. It is generally safe to use an inexpensive drum core or "open field" type inductor in this application. The output noise filter capacitor,  $C$ , should have low ESL and ESR but does not handle much ac ripple current.

Be careful in applying pi output filters as they generally degrade output load transient response. If the filter is placed inside the feedback loop, compensation will be tricky. The pi filter can be equally effective when used on the output of a buck-boost converter.

## Capacitor Functions in Buck Converter



- ◆  $C_{IN}$  must handle high discontinuous ripple current. ESR, ESL should be low.
- ◆  $C_{OUT}$  has continuous ripple current and must minimize output ripple voltage. ESR should be low.
- ◆  $C_{OUT}$  affects loop stability and load step transient response.

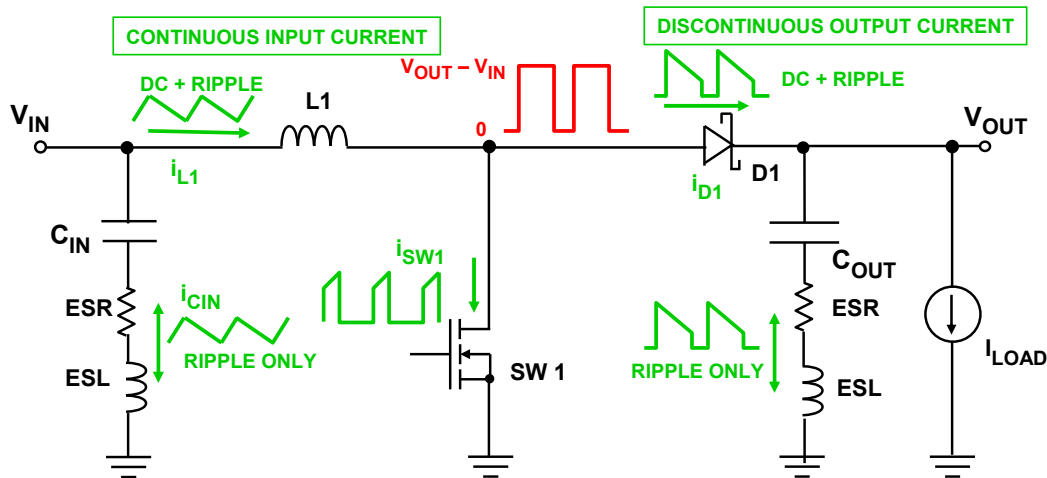
The input ripple current waveform of a buck converter is discontinuous with high  $di/dt$  and peak-to-peak amplitude. The input capacitor supplies pulse currents to the upper MOSFET. The input capacitor must therefore have high ripple current handling capability and low inductance. It is usually unwise to allow this input ripple current to be handled by other, uncontrolled bypass capacitors in the system. An inductor is sometimes placed in series with the input supply line capacitor to provide further filtering.

Output ripple current in a buck converter is continuous and usually low, so capacitor ripple current ratings are not usually an issue. However, buck regulators are commonly used to power loads such as processor cores and FPGAs which can impose severe dynamic load regulation requirements. When processor core output voltages approach 1 volt, the allowed error band is proportionately small (50 mV for 5% error), so a controlled low impedance over a broad frequency range is required.

The output capacitor is an integral part of closed loop stability of the buck converter. It smoothes the ripple current coming out of the converter, reducing the ripple voltage. The output capacitor supplies current during transient conditions until the feedback loop acts to increase the inductor current.

A good design tool, such as ADIsimPower, calculates the ripple current in the capacitors and inductors and makes the appropriate parts selection.

## Capacitor Functions in a Boost Converter



- ◆  $C_{IN}$  filters continuous ripple current and stabilizes feedback loop.
- ◆  $C_{OUT}$  filters discontinuous output ripple current and must minimize output ripple voltage. ESR should be low.
- ◆ Pi-Filter on output often less costly than optimizing  $C_{OUT}$ .
- ◆  $C_{OUT}$  affects loop stability and load step transient response.

As previously discussed, the boost converter has continuous input current and discontinuous output current. The input capacitor smoothes the ripple current going into the converter, reducing the ripple voltage on the input. The input capacitor also provides low impedance on the input to ensure stability.

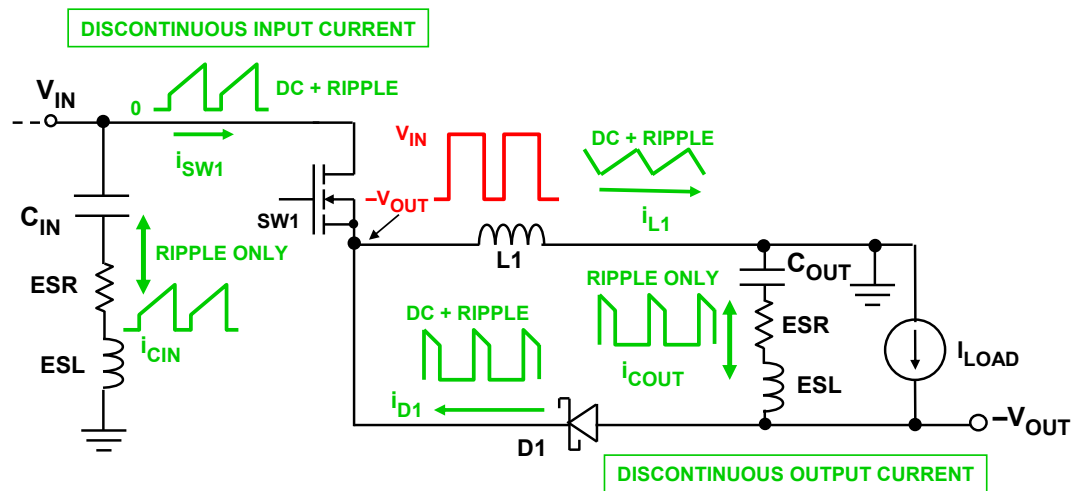
The output capacitor is an integral part of closed loop stability of the boost converter. It must supply the load current when the MOSFET is on and the diode is off.

Output capacitor also supplies current during load transient conditions until the feedback loop responds and increases the inductor current.

Depending upon the capacitor technology, an output filter that is designed to handle the high ripple current will tend to produce high output ripple voltage. An output filter that is designed to produce the desired ripple voltage is likely to be significantly larger and more expensive. So boost converters often use a pi filter in the output to more efficiently filter the output ripple voltage.



## Capacitor Functions in Buck-Boost Regulators

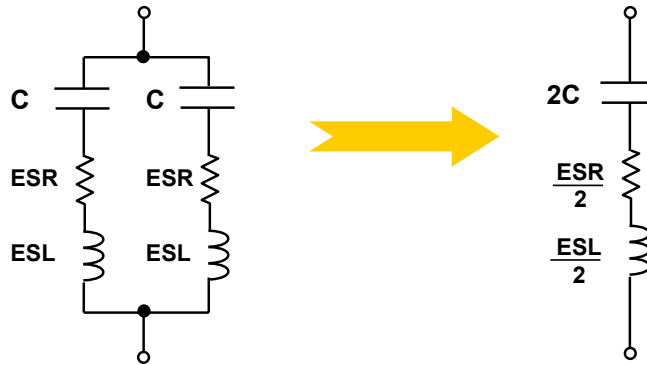


- ◆ Large discontinuous input and output ripple current with high  $di/dt$ .
- ◆ Often requires a pi filter on the output to control ripple.

In terms of input/output ripple current, the buck boost converter offers the worst of both worlds—large discontinuous ripple current with high  $di/dt$  on both the input and output, both must be handled by their respective filter capacitors.

Like the boost converter, the buck-boost converter is often used with a pi filter on the output, instead of the simple “L” section shown here.

## Parallel Capacitors



- ◆ **Twice the capacitance, half the ESR, half the ESL**
- ◆ **Sometimes more cost effective than trying to do it with a single capacitor**
- ◆ **Sometimes the only way to get required C and ESR to meet ripple requirements**
- ◆ **May increase real estate, but depends highly on type of capacitor**
- ◆ **Bulk capacitors may be composed of several parallel capacitors, sometimes of different values**

Output capacitors are often used in parallel combinations of multiple individual capacitors. Parallel capacitors have a total capacitance equal to the sum of all their individual values.

An added benefit is that the effective ESR and ESL is reduced since the impedance of paralleled resistors goes according to the formula:

$$\frac{1}{Z_T} = \frac{1}{Z_1} + \frac{1}{Z_2} + \dots + \frac{1}{Z_x}$$

In some cases parallel capacitors provide a more cost effective solution than trying to use a single capacitor. Sometimes parallel capacitors are the only way to get the required C and ESR to meet the ripple requirements.

It is a common practice to parallel different types and values of capacitors to take advantage of the low ESR and ESL of ceramic capacitors, while having the benefit of large capacitance values of aluminum or "bulk" capacitors. However, when you parallel different types of capacitors, you can't simply add the C value and parallel the ESR and ESL values. The resulting impedance must be calculated based on the complex impedance model.

## Popular Capacitor Types

TECHNOLOGY	ADVANTAGES	DISADVANTAGES	APPLICATIONS
Aluminum Electrolytic (Switching Type)	<ul style="list-style-type: none"> <li>•High CV product/cost</li> <li>•Large energy storage</li> <li>•Best for 100V to 400V</li> </ul>	<ul style="list-style-type: none"> <li>•Temperature related wearout</li> <li>•High ESR/size</li> <li>•High ESR @ low temp</li> </ul>	<ul style="list-style-type: none"> <li>•Consumer products</li> <li>•Large bulk storage</li> </ul>
Solid Tantalum	<ul style="list-style-type: none"> <li>•High CV product/size</li> <li>•Stable @ cold temp</li> <li>•No wearout</li> </ul>	<ul style="list-style-type: none"> <li>•Fire hazard with reverse voltage</li> <li>•Expensive</li> <li>•Only rated up to 50V</li> </ul>	<ul style="list-style-type: none"> <li>•Popular in military</li> <li>•Concern for tantalum raw material supply</li> </ul>
Aluminum-Polymer, Special-Polymer, Poscap, OsCon	<ul style="list-style-type: none"> <li>•Low ESR</li> <li>•Z stable over temp</li> <li>•Relatively small case</li> </ul>	<ul style="list-style-type: none"> <li>•Rapid degradation above 105°C</li> <li>•Relatively high cost</li> </ul>	<ul style="list-style-type: none"> <li>•Newest technology</li> <li>•CPU core regulators</li> </ul>
Ceramic	<ul style="list-style-type: none"> <li>•Lowest ESR, ESL</li> <li>•High ripple current</li> <li>•X7R good over wide temp</li> </ul>	<ul style="list-style-type: none"> <li>•CV product limited</li> <li>•Microphonics</li> <li>•C decreases with increasing voltage</li> </ul>	<ul style="list-style-type: none"> <li>•Excellent for HF decoupling</li> <li>•Good to 1GHz</li> </ul>
Film (Polyester, Teflon, polypropylene, polystyrene, etc.	<ul style="list-style-type: none"> <li>•Hi Q in large sizes</li> <li>•No wearout</li> <li>•High voltage</li> </ul>	<ul style="list-style-type: none"> <li>•CV product limited</li> <li>•Not popular in SMT</li> <li>•High cost</li> </ul>	<ul style="list-style-type: none"> <li>•High voltage, current</li> <li>•AC</li> <li>•Audio</li> </ul>

This is a survey of some of the more popular capacitor types. Note that not all values are available in all types, and the physical size can vary widely for the same value of capacitance.

## Aluminum Electrolytic Capacitors



- ◆ Aluminum electrolytic capacitors provide large capacitance (100µF to > 1mF) in relatively small size at very low cost
- ◆ Represent the best µF/cost of all options
- ◆ Achieve this with high dielectric constant ( $\epsilon$ ) due to oxide film, and thin layers, (d is small)
- ◆ High ESR: can be several ohms
- ◆ Aging due to dry-out must be taken into account in long lifetime designs
- ◆ Surface mount available, but some reliability issues. Other technologies better for lower capacitance values
- ◆ Poor high frequency performance
- ◆ Use "switching" types, not "general purpose" in switcher designs

Switching type aluminum electrolytic capacitor are designed and constructed for use in SMPS. They have lower ESR and ESL than general purpose aluminum capacitors, generally meaning higher ripple current. "General purpose" aluminum electrolytic capacitors should not be used in switcher designs.

Aluminum electrolytics are available in large values and in relatively small size and low cost. This is accomplished by using an oxide film with high dielectric constant and thin layers.

The chief disadvantage of aluminum electrolytics is the high ESR, which can be several ohms.

Because of their poor high frequency performance, they are often paralleled with other types of capacitors to achieve the desired filtering characteristic.

## Solid Tantalum Capacitors



- ◆ A type of solid electrolytic capacitor, using tantalum powder as dielectric
- ◆ Size efficient for 10's of  $\mu\text{F}$  range
- ◆ Capacitance is temperature stable
- ◆ ESR is in the range of 100's of  $\text{m}\Omega$ , lower than aluminum electrolytics
- ◆ Must be designed for  $2 \times$  voltage rating
- ◆ Safety is a concern (e.g. reverse polarity, overvoltage rating): as failure is seen as burn out of capacitor with flame
- ◆ Popular in high-rel military applications
- ◆ However, becoming less popular, as ceramic capacitors can achieve same capacitance with lower ESR, and ESL, and less safety issues without cost penalty

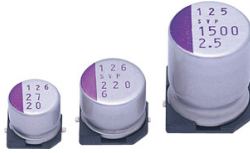
Solid tantalum capacitors have traditionally been popular in small hand held devices and in servers, but recent polymer and ceramic capacitor improvements have made tantalum less attractive.

Raw material sourcing issues have also reduced tantalum's market share (increased price).

Extreme care must be taken with tantalum capacitors to avoid reverse voltage or overvoltage, as these conditions can cause the capacitor to burn out.

In spite of these concerns, tantalum capacitors are highly reliable and have been very popular in military applications. However, modern ceramic capacitors can achieve nearly the same capacitance with lower ESR and ESL and are replacing tantalums in many applications.

Only solid tantalum capacitors should be considered in modern applications. The "wet slug" type tantalum capacitors are not suitable in today's designs.



## OS-CON (Sanyo)



- ◆ Offers large capacitance and very low ESR in relatively small package with > 16V rating
- ◆ Useful for generating 100 $\mu$ F or more capacitance, and maintaining ESR of < 50 m $\Omega$  (5 m $\Omega$  available)
- ◆ Can handle 0.5 to 4A of RMS ripple current
- ◆ Suitable for high current designs requiring very low voltage ripple
- ◆ > 5000 hours at 105°C with capacitance remaining within  $\pm 20\%$ , with some ESR increase
- ◆ Suitable for long lifetime products
- ◆ Lowest Height 4mm
  - Not suitable for portable designs
  - Used a great deal in servers, CPU voltage regulators
- ◆ Cost \$0.50 to \$1.00/100k piece price

OS-CON capacitors are attractive due to their reduced ESR and ESL. "OS-CON" is a trademark of Sanyo and stands for "organic semiconductor."

OS-CON is an aluminum solid capacitor with high conductive polymer or organic semiconductor electrolyte material. OS-CON achieves low Equivalent Series Resistance (ESR), excellent noise reduction capability and frequency characteristics. In addition, OS-CON has a long life span, and its ESR has little change even at low temperatures since the electrolyte is solid.

Other companies such as United Chemi-con have come out with similar products based on an aluminum polymer technology that may have slightly lower lifetime but are more cost effective for the same capacitance and similar ESR.

## **POSCAP (Polymer Organic Semiconductor Capacitor)**



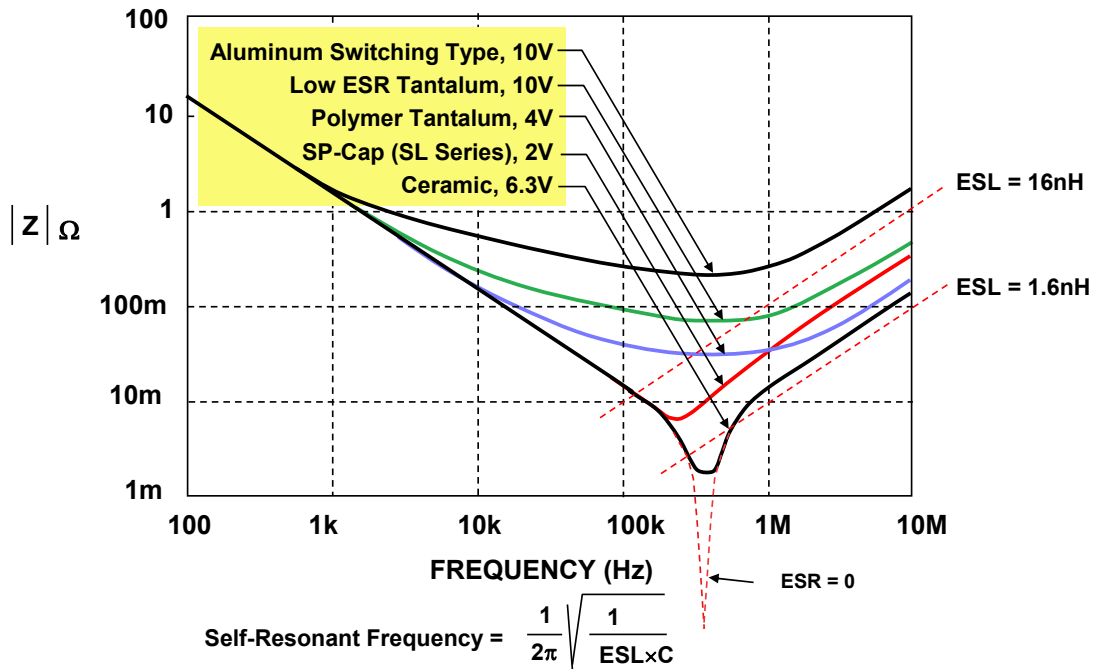
- ◆ Solid electrolytic capacitor with Sanyo-specific organic compound
- ◆ Offers reasonably low ESR (50mΩ down to 5mΩ)
- ◆ Small Size and Height
- ◆ Values up to 1000μF available
- ◆ Generally low voltage (up to 25V but limited capacitance)
- ◆ Cost 47μF, 6.3V: \$0.40 to \$1.50 at 100k piece price
  - Less expensive than similar specified ceramic
  - More expensive than similar standard electrolytic or tantalum

This capacitor type is similar to the OS-CON and also made by Sanyo.

"POSCAP" is a solid electrolytic chip capacitor. The anode is sintered tantalum, and the cathode is a highly conductive polymer. "POSCAP" has a low ESR and excellent performance at high frequency with a low profile and high capacitance. In addition, it has high reliability and high heat resistance.

Panasonic also has a "Special Polymer" cap that has similar specifications in the same footprint as the "POSCAP." The cost is also comparable for similar values.

## Impedance of Various 100μF Capacitors



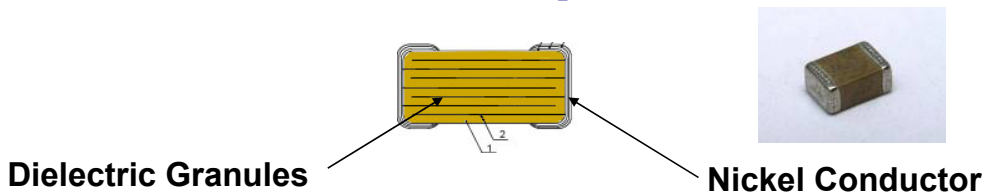
This is a graph adapted from Panasonic's "S-P Capacitor Technical Guide" showcasing their "Special Polymer" capacitor technology. It may cast a slightly unfavorable light on their competitor's product (namely Polymer Tantalum) but it shows the general trend of various capacitor types.

General purpose aluminum electrolytics have slightly higher ESR than the switching type. However, they are not recommended for switching supply applications.

As you can see here, the ceramic capacitor has the lowest ESR at the switching frequency and the lowest ESL.



## Ceramic Capacitors



- ◆ Multilayer ceramic capacitors (MLCC) offer extremely low ESR ( $<10\text{m}\Omega$ ) and ESL ( $<1\text{nH}$ ) in a small thin package
- ◆ "0603" is  $1.6\text{mm (l)} \times 0.8\text{mm (w)} \times 0.8\text{mm (h)}$
- ◆ Best cost for performance from  $1\text{pF}$  to  $40\mu\text{F}$ 
  - Most suitable capacitor for portable power, decoupling supplies
  - Available up to  $100\mu\text{F}$ , but become larger and more expensive above  $10\mu\text{F}$
  - Cost is dependent on value, with lower values being cheaper due to less layers being printed. More popular values cheaper.
  - $1\mu\text{F}$   $16\text{V}$ , 0603 is  $< \$0.01$  in 100k pieces
- ◆ Resilient to fault conditions – voltage surges etc.
- ◆ Capacitance value decreases with increasing voltage (stick with X7R types for best results)

Due to low ESR, ceramic capacitors can handle very high ripple currents for their size. They are exclusively used in compensation and small signal circuits, and are very good for reducing ripple voltage on the input and output of switching supplies. Their ESL is also low, making them good choices at high frequencies.

Due to their limitation in upper capacitance value, they are often paralleled with other capacitor types on the input and output of switching supplies.

The ESL of a standard multilayer ceramic capacitor in an 0603 case is approximately  $1\text{ nH}$ .

Other more expensive ceramic technologies are available which can reduce the ESL to less than  $100\text{ pH}$ .

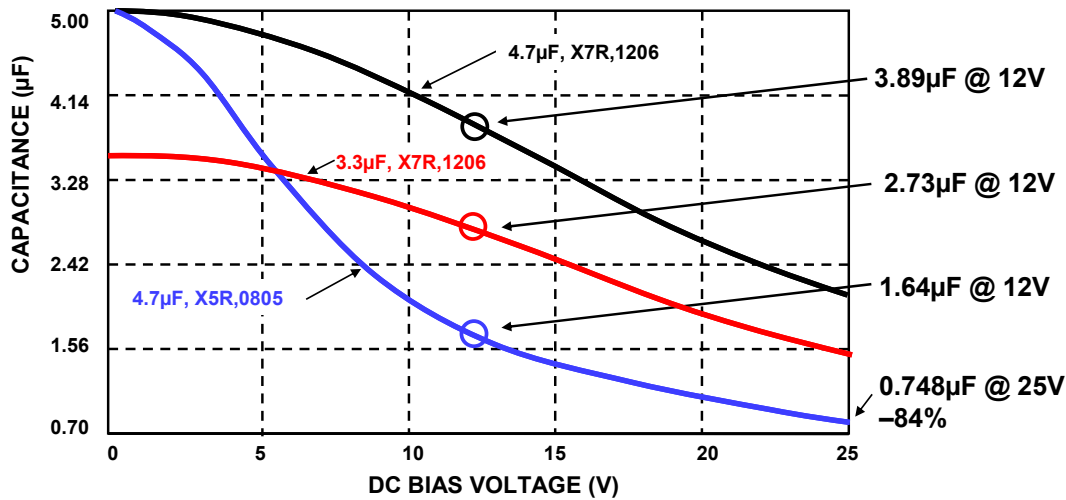
One type is the low inductance chip capacitor (LICC) which has a reverse-geometry where the terminations are located on the long sides rather than the short sides of the rectangular package.

Other low inductance types are the inter-digitated capacitors (IDC), land grid array (LGA) capacitors, and low-inductance capacitor arrays (LICA).

Details of these low inductance capacitors can be found at the AVX website, [www.avxcorp.com](http://www.avxcorp.com), and in the following reference:

Tim Sullivan, "Choosing Decoupling Capacitors," *Electronic Products*, December 2007, available at [www.electronicproducts.com/ShowPage.asp?FileName=farr\\_avx\\_dec2007.html](http://www.electronicproducts.com/ShowPage.asp?FileName=farr_avx_dec2007.html).

## Which Ceramic Capacitor Provides More Capacitance?



- ◆ Generally more temperature stable parts (X7R) have less variation due to applied voltage

A potential problem with ceramic capacitors is their capacitance change with dc bias voltage. This may or may not be a problem in decoupling applications, but it can be a real issue if the capacitor is used in a critical compensation network, for example. Another place where the voltage coefficient is a problem is where the capacitor is used in the signal path, and the signal modulates the voltage. This can produce unwanted harmonics because of the signal-dependent capacitance.

These plots show capacitance versus applied dc bias voltage for three types of ceramic capacitors:

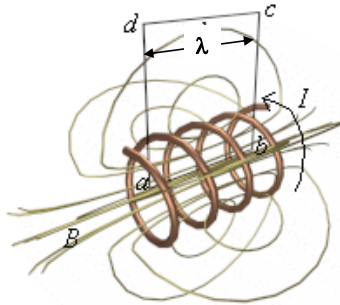
- 4.7 µF, 25V, X7R, 1206 case style
- 4.7 µF, 25 V, X5R, 0805 case style (higher K, smaller case)
- 3.3 µF, 25 V, X7R, 1206 case style

It is interesting that the 3.3 µF (at zero bias) X7R capacitor actually has a larger capacitance at 12 V bias than the 4.7 µF X5R type. At full rated voltage, the X5R capacitor is down 84% from its zero bias value. Note that the X7R capacitors (which have a slightly lower dielectric constant) maintain their capacitance better with dc bias voltage than the X5R type.

In addition, the X7R types perform better over temperature and should be used in preference to the X5R. Avoid using Z5U and Y5V types which are worse.

## Inductor Basics

- ◆ An inductor is a magnetic energy storage element which consists of a conducting coil surrounding a core, usually made of ferrite material or powdered iron



$$L(\text{Henries}) = \frac{\mu \cdot n^2 \cdot A}{\lambda}$$

$\mu$  = permeability of core,  
 $n$  = number of turns,  
 $A$  = cross-sectional area of core,  
 $\lambda$  = effective length of core

- ◆ Air:  $\mu = 1.257 \times 10^{-6}$  H/m
- ◆ Ferrite U M33:  $\mu = 9.42 \times 10^{-4}$  H/m
- ◆ Nickel:  $\mu = 7.54 \times 10^{-4}$  H/m
- ◆ Iron:  $\mu = 6.28 \times 10^{-3}$  H/m
- ◆ Ferrite T38:  $\mu = 1.26 \times 10^{-2}$  H/m
- ◆ Silicon GO steel:  $\mu = 5.03 \times 10^{-2}$  H/m
- ◆ Superalloy:  $\mu = 1.26$  H/m

- ◆ Larger core cross-sectional area, coil turns and/or core permeability increase inductance

The practical inductor consists of a conductor coil wound on a ferromagnetic core. This combination yields an inductance ( $L$ ) that offers a reluctance to a change in current, and therefore the current through an inductor cannot change instantaneously.

The rate of change of current through an inductor ( $di/dt$ ) is determined by the inductance and the voltage dropped across the inductor, given by the expression:

$$v = L \times di/dt.$$

The use of ferromagnetic material as the inductor core allows energy to be stored in the inductor. When a positive voltage is applied to the inductor, the current increases, and energy is added to the inductor magnetic field.

The inductive impedance can be calculated from:

$$Z_L = j\omega L$$

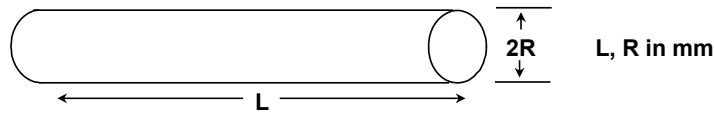
where:

$$j = \sqrt{-1}$$

and

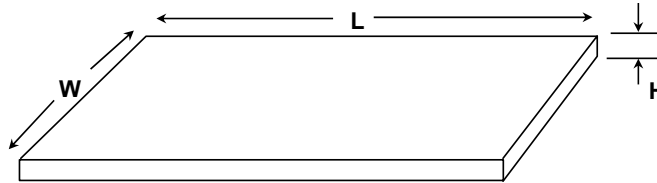
$$\omega = \text{radian frequency} = 2\pi \times \text{frequency in Hertz}$$

## Wire and Strip Inductance Calculations



$$\text{WIRE INDUCTANCE} = 0.0002L \left[ \ln \left( \frac{2L}{R} \right) - 0.75 \right] \mu\text{H}$$

**EXAMPLE:** 1cm of 0.5mm o.d. wire has an inductance of 7.26nH  
(2R = 0.5mm, L = 1cm)



$$\text{STRIP INDUCTANCE} = 0.0002L \left[ \ln \left( \frac{2L}{W+H} \right) + 0.2235 \left( \frac{W+H}{L} \right) + 0.5 \right] \mu\text{H}$$

**EXAMPLE:** 1cm of 0.25 mm PC track has an inductance of 9.59 nH  
(H = 0.038mm, W = 0.25mm, L = 1cm)

A piece of wire or a PCB trace will have inductance, even though it is not a coil.

In addition to the resistance (basically a dc spec), a trace (wire or ground plane) will have a frequency dependent impedance component (known as inductance).

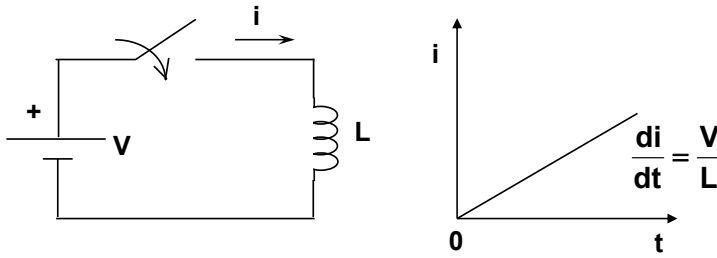
Inductive impedance increases linearly with frequency. This can become significant at higher frequencies.

The above figure shows simple equations to calculate the inductance of a length of wire or a rectangular strip conductor. The assumption is that the return current path is a fairly long distance away from the wire or strip—the wire or strip is treated as a circuit element.

However, on a PCB the actual inductance also depends on the loop area which includes the current return path, and the above equations are no longer valid. There are modeling packages available to determine the actual trace impedance in these cases.

For example, the effective inductance of a gate drive trace may be as much as a factor of 10 lower than predicted by the above equation if it runs directly over a ground plane.

## Inductor Basic Current/Voltage Relationship



$$E(\text{joules}) = \frac{1}{2} \cdot L \cdot i^2$$

- ◆ Inductor current increases at rate of  $V/L$
- ◆ If inductor current tries to change rapidly (switch opened), a large voltage will be generated as the magnetic field collapses
- ◆ Energy stored is proportional to the inductance and the square of the current.

You cannot change the current through an inductor instantaneously. When a voltage is applied to the inductor, the current increases, and energy is added to the inductor magnetic field. When the switch is opened, the inductor current goes to zero, and a large voltage is generated as the magnetic field collapses.

The inductor magnetic field can only hold a finite amount of energy before the ferromagnetic material will saturate. Saturation causes the inductance to decrease and ripple current to increase in a switching supply. When making an inductor selection, it is important to check that the core saturation current ( $I_{SAT}$ ) is greater than the application's peak inductor current,

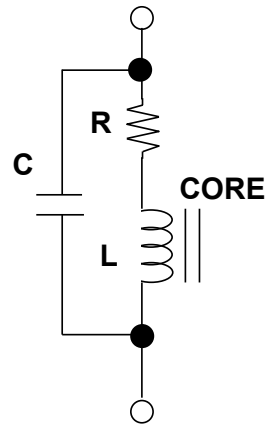
$$(I_{PEAK} = I_{OUT} + I_{RIPPLE}/2).$$

## Inductor Model

**IDEAL**



**ACTUAL MODEL  
(APPROXIMATE)**



Just as with the capacitor, a real inductor will have a more complex model.

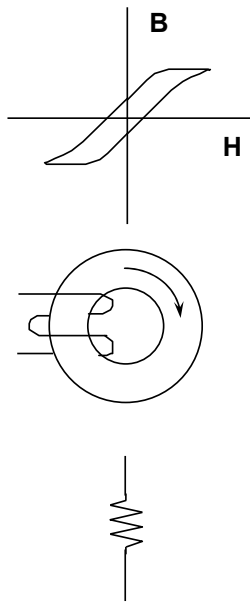
The inductor will have series resistance (called DCR for dc resistance) just as in a capacitor. There is also a small amount of parallel parasitic capacitance which can be relevant in RF applications.

Another consideration is the inductor self-resonant frequency. A practical example would be an inductor of 10  $\mu\text{H}$  which has an equivalent distributed capacitance of 5 pF. The self-resonant frequency can be calculated as follows:

$$f_{\text{resonance}} = \frac{1}{2\pi} \sqrt{\frac{1}{LC}} = 22.5 \text{ MHz}$$

The switching frequency of the regulator should be at least ten times less than the inductor self-resonant frequency. In most practical designs with switching frequencies less than 2 MHz this will be the case, but a quick calculation is a good idea.

## Inductor Power Losses



LOSS	FUNCTION OF
Magnetic Hysteresis	<ul style="list-style-type: none"> <li>◆ Core Material</li> <li>◆ Core Volume</li> <li>◆ Flux Density</li> <li>◆ Frequency</li> </ul>
Eddy Currents	<ul style="list-style-type: none"> <li>◆ Core Material</li> <li>◆ Core Volume</li> <li>◆ Flux Density</li> <li>◆ Frequency</li> </ul>
Winding Resistance	<ul style="list-style-type: none"> <li>◆ Wire Size</li> <li>◆ Number of Turns</li> <li>◆ Core Volume</li> </ul>

◆ **Figure of Merit: "Q"** =  $\frac{2\pi fL}{R}$

Another important consideration is that the temperature of the inductor will rise due to internal power losses. The designer needs to consider winding resistance loss (sometimes referred to a copper loss) and core losses from eddy currents (often referred to a core loss).

Winding resistance power loss is due to the effective current ( $I_{RMS}$ ) flowing through the resistance ( $R_{DC}$ ) of the conductor winding, simply expressed as:

$$P_{CU} = R_{DC} \times I_{RMS}^2.$$

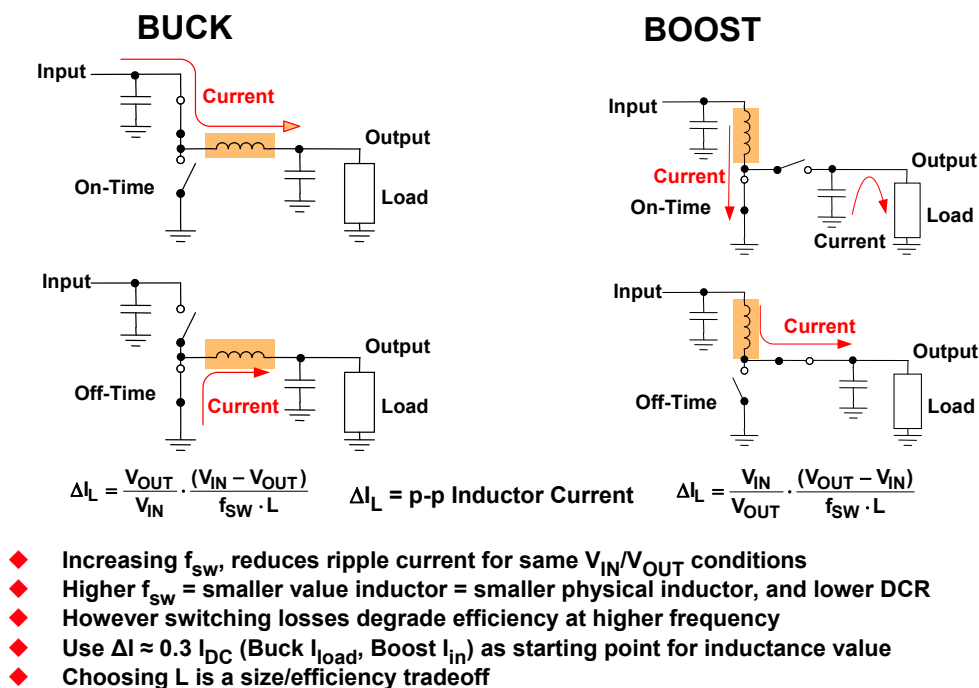
Inductor data sheets typically specify a temperature rise at a given current—for example, the equivalent dc current yielding a 40°C temperature rise. The lower value of the temperature rise and saturation current is called the "rated" current of the inductor.

The mechanism of core loss is more complex. Recall that current flowing through an inductor winding induces a magnetic flux in the ferromagnetic material, or the core. So the changing current in the power inductor generates a changing flux density ( $B_{AC}$ ) and the reluctance of the core material tends to oppose this  $B_{AC}$ .

Just like the current flowing through the conductor results in copper losses due to the conductor's resistance to the flow of current, the core's reluctance to a changing flux generates a core loss. The core loss is determined by the type of core material, the amount of material, the  $B_{AC}$ , and the frequency of change, that is, the switching frequency ( $F$ ). A good power inductor data sheet will simplify this equation based on a calculated  $B_{AC}$  for the operating condition of the inductor and the core material and size.

While the data sheet may specify a temperature rise current, it is important to note that where the core losses are significant, the inductor will reach the specified temperature rise at lower rms current because of the additional temperature rise caused by the core loss.

## Inductor Functions in Switching Converters



The primary function of an inductor in a switch mode power supply is to act as an energy storage device. Another function of the inductor is to act as a filter—either on the input or output or both.

This figure reviews the basic operation of a buck and boost converter and how the inductor acts to step down (buck) or step up (boost) the input voltage.

The calculation of the required inductor value begins by determining the maximum peak-to-peak ripple current,  $\Delta I_L$ . This value is typically chosen to be about 30% of the output dc load current for a buck converter, and 30% of the input dc current for a boost converter.

The inductor value itself can then be found by solving the above equations for L, given the value of  $\Delta I_L$ ,  $V_{IN}$ ,  $V_{OUT}$ , and  $f_{SW}$ .

Note that increasing the switching frequency reduces the value of the inductor required for the same ripple current.

The ADIsimPower design tool calculates the proper value for the inductor based on the customer requirements as well as determines the exact part and manufacturer for use in the bill of materials.

The ADIsimPower vendor database contains over 4000 individual parts. The inductor core loss data has been included in the inductor model and is not generally published by the manufacturer.



## Inductor Specifications

Part number	L <sup>1</sup> ( $\mu$ H)	Percent tol	DCR <sup>2</sup> max (Ohms)	SRF <sup>3</sup> typ (MHz)	I <sub>sat</sub> <sup>4</sup> (A)	I <sub>rms</sub> <sup>5</sup> (A)
DO3316P-682_L_	6.8	20,10	0.027	38	4.6	4.4
DO3316P-103_L_	10	20,10 20	0.038	30	3.8	3.9

1. **Inductances** may vary 20 to 30% from the nominal inductor value! Current ripple could be increased 43%. Coilcraft offers 10% and 20% tolerance.
2. **DCR**: DC resistance. Physically smaller inductors (for same L) will have larger DCR due to reduced wire thickness and increased efficiency losses.
3. **SRF**: Resonant frequency of inductor and parasitic capacitance of inductor—typically not a concern for design.
4. **I<sub>sat</sub>**: Inductor current level for which the inductance falls 10% using coilcraft, for others it is –30%! You don't want to operate at –30% (–10% is OK)
5. **I<sub>rms</sub>** (Also called I<sub>max</sub>): At this RMS current level the temperature of the inductor will rise 40°C. Inductors are usually rated to 125°C. Typically you don't want to have inductor rising much more than 40°C, because saturation current level is further decreased.

This figure shows specifications for a particular inductor taken from the manufacturer's data sheet (in this case, Coilcraft).

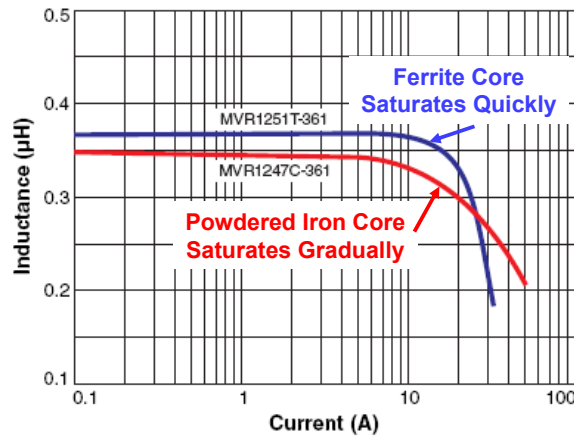
The inductance value can vary 20% to 30% from the nominal value, however, Coilcraft offers 10% and 20% tolerances. Since inductor ripple current is inversely proportional to L, inductances less than nominal will cause an increase in ripple current.

Another important specification is the saturation current, I<sub>sat</sub>, which is the inductor current level for which the inductance falls 10% (Coilcraft inductors). For other manufacturers, it is –30%.

Operation at 10% saturation is acceptable provided it represents the maximum load and worst case conditions. Knowing this is valuable in selecting the right inductor value. Inductors which are larger than necessary take up more real estate and are more expensive.

The specification I<sub>rms</sub> (or I<sub>max</sub>) is the rms current level at which the temperature of the inductor will rise 40°C. The maximum allowable temperature is usually 125°C. If you allow the inductor temperature to rise more than 40°C the saturation current level will probably be further decreased.

## Inductor Cores and Their Characteristics



- ◆ Natural air gaps in powdered iron core cause a more gradual saturation curve for same physical size.
- ◆ Powdered iron cores suited to applications requiring large instantaneous current (i.e., camera flash, VRM power supplies).
- ◆ Powdered iron cores more expensive and have higher core losses.

There are two basic types of cores commonly used for inductors: powdered iron and solid ferrite.

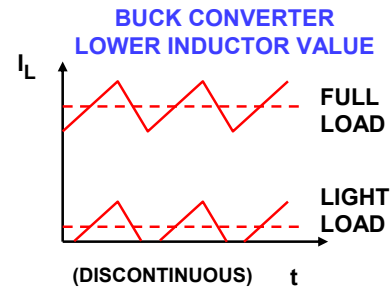
The powdered iron core has natural air gaps which cause a more gradual saturation curve for the same physical size (compared to solid ferrite cores). Because of the gradual saturation, powdered iron cores are more suited to applications requiring large instantaneous currents such as camera flash and VRM power supplies.

Ferrite core inductors saturate quickly but are lower cost and have lower core losses. They are therefore more suited for standard POL switching supplies.

## Inductor Selection Considerations

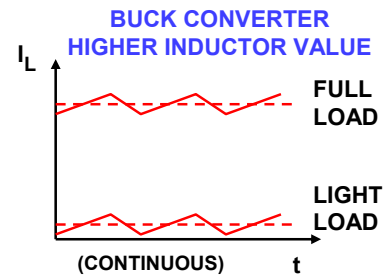
### ◆ Benefits of low value inductors

- Lower DCR
- Higher saturation current
- Higher  $di/dt$
- Faster switching frequencies
- Improved transient response
- Less output capacitance required for given transient performance



### ◆ Benefits of high value inductors

- Lower ripple current
- Lower AC loss (skin effect, hysteresis)
- Lower RMS current in switches
- Lower RMS capacitor current (mainly output)
- Continuous inductor current over wider load range
- Less capacitance required for an equivalent output ripple

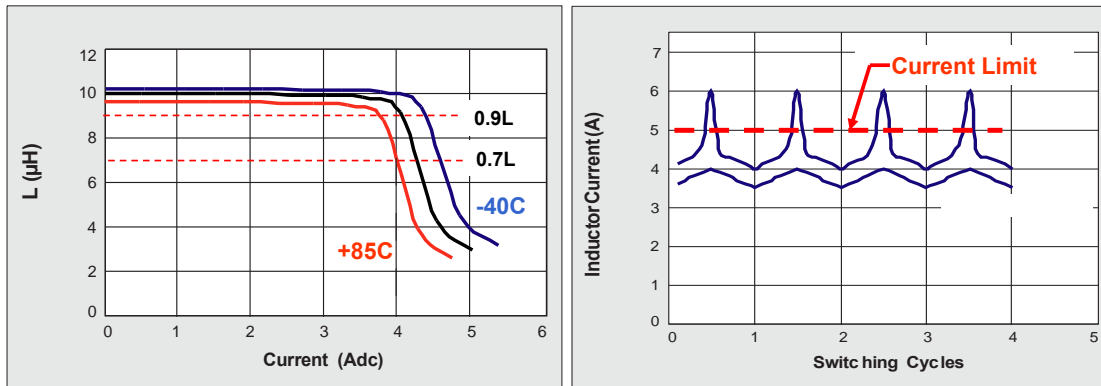


This figure examines the tradeoffs between low and high value inductors. The ultimate choice depends on the particular design.

The ADIsimPower design tool strives to achieve the desired performance with the lowest practical inductor. This philosophy is the proper one for most modern portable systems.

On the other hand, higher value inductors do have certain advantages as shown in the figure. Under certain conditions they may be the desirable choice.

## Saturation of Inductors



- ◆ The inductor core can become biased with too much current resulting in a sudden drop in inductance.
- ◆ Operating with  $I_{\text{DC}} + \Delta I / 2$  equal to a current  $I_{\text{SAT}}$  which causes a 30% drop in  $L$  will cause issues:
  - Ripple current increase > 40%
  - May hit current limit for lower DC current than desired
  - Core saturation results in core efficiency loss
  - Greater  $di/dt$  results in increased EMI leakage
- ◆ Over designing will result in physically large inductors
  - 10% saturation for peak current at maximum load and worst case conditions is a reasonable compromise. For the above example, this would be about 4A.
  - Check Inductor saturation curves vs. temperature—Don't just read spec!

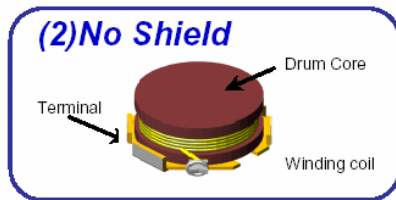
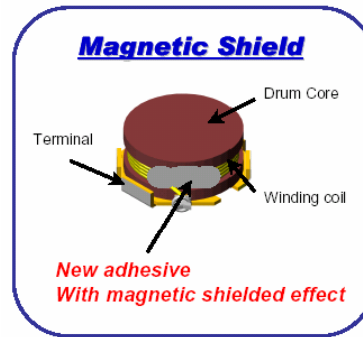
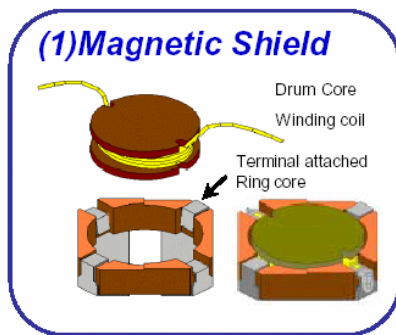
This figure shows what happens to the inductor ripple current when the saturation current ( $I_{\text{sat}}$ ) is exceeded. Exceeding the saturation current causes a sudden drop in inductance and a corresponding rise in the inductor current.

The saturation current ( $I_{\text{sat}}$ ) is the current at which the inductance drops by a maximum of 10% below the lower limit of its value specified at 0 A dc bias. This is the definition Coilcraft uses. Other manufactures use different percentages.

The inductance at  $I_{\text{sat}}$  is measured at the specified ambient temperature by applying dc bias for a short period of time to minimize self-heating.

Selecting the inductor such that it will reach 10% saturation for peak current at maximum load and worst case conditions is a good compromise. For the example shown in the figure, this would be about 4 A.

## Shielded or Unshielded?



- ◆ Shielded inductors reduce EMI and potential interference
- ◆ RF designs almost always use shielded inductors
- ◆ Manufacturing cost is higher
- ◆ Current rating per mm<sup>2</sup> is reduced

Model	L, $\mu$ H	DCR, $\Omega$	SRF, MHz	ISAT, A	IRMS, A	Shielded	Size, mm	Price, \$ 1k
DO5022P-103ML	10	0.031	30	10	4.3	No	18 x 15	0.73
DS5022P-103ML	10	0.04	30	8	3.9	Yes	18 x 15	1.11

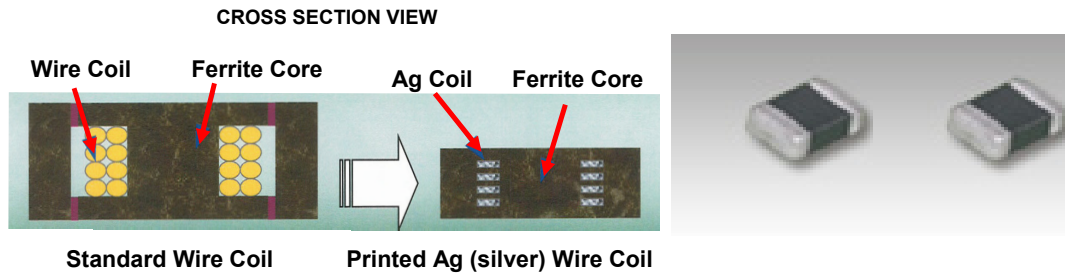
To shield or not to shield, that is the question.

Shielding will reduce EMI. Although the cost will increase slightly, as is shown in the figure. Shielding will tend to lower the saturation current, which in turn lowers the maximum allowable rms current.

Shielded inductors are very common in RF applications.

The above figure compares two similar inductors from Coilcraft. Both are the same size and value, but the shielded version has slightly lower Isat and Irms currents.

## **New Inductor Technology: Multilayer Ceramic Inductors for Power**



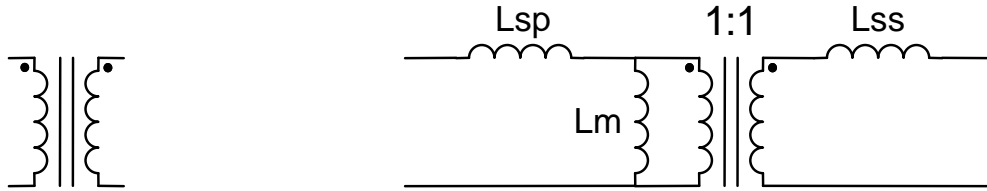
- ◆ **Characteristics of Ceramic Inductors**
  - **Low cost (about 50% to 65% of coil types with similar specifications)**
  - **Small size (2.5mm x 2.0mm x 1mm(h), 1.5μH,  $I_{SAT} = 1.5A$ )**
  - **Lower DCR improves efficiency**
  - **Useful < 2.2μH (drives IC manufacturers to higher switching frequencies)**
  - **$I_{max} = 1.5A$  due to small printed Ag (silver) wire coils**
  - **Usable to about 1.0A due to saturation**
- ◆ **Manufacturers: FDK, Murata, TDK, Toko (in development)**

Multilayer ceramic inductors lower cost, smaller size, lower DCR than standard wire coil inductors. The only disadvantage is that the saturation current is typically limited to about 1.5 A because of the small printed silver wire coils.

The upper range of inductance is limited to a few microhenries.

## Coupled inductors

- ◆ A coupled inductor is an inductor with multiple windings on the same core
- ◆ Coupled inductors are basically transformers with poor coupling and low magnetizing inductance
- ◆ A flyback transformer could be considered a coupled inductor with good coupling



Ideal Transformer

Coupled Inductor Model

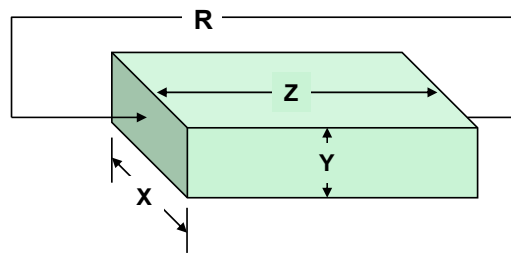
A coupled inductor is an inductor with multiple windings on the same core. It is similar to a transformer but has more losses and a more complex model. It can be viewed as a transformer with poor coupling and low magnetizing inductance.

This figure shows the relationship between the ideal transformer and a coupled inductor. The 1:1 transformer in the model is an ideal transformer (all it does is offer isolation)

The coupled inductor is more complex, since no simplifications can be made to the circuit model. Coupled inductors generally have a 1:1 turns ratio, so  $L_{sp} = L_{ss}$ .

Often  $L_m$  is of the same order of magnitude as  $L_{sp}$  and  $L_{ss}$ .

## Calculation of Sheet Resistance and Linear Resistance



$$R = \frac{\rho Z}{XY}$$

$\rho$  = RESISTIVITY

### SHEET RESISTANCE CALCULATION FOR 1 OZ. COPPER CONDUCTOR:

$$\rho = 1.724 \times 10^{-6} \Omega \text{ cm}, Y = 0.0036 \text{ cm}$$

$$R = 0.491 \frac{Z}{X} \text{ m}\Omega$$

$$\frac{Z}{X} = \text{NUMBER OF SQUARES}$$

$$R = \text{SHEET RESISTANCE OF 1 SQUARE (Z = X)} \\ = 0.491 \text{ m}\Omega / \text{SQUARE}$$

We will now examine the resistor, another passive component.

All conductors have some resistance (at least when operating above 0°K).

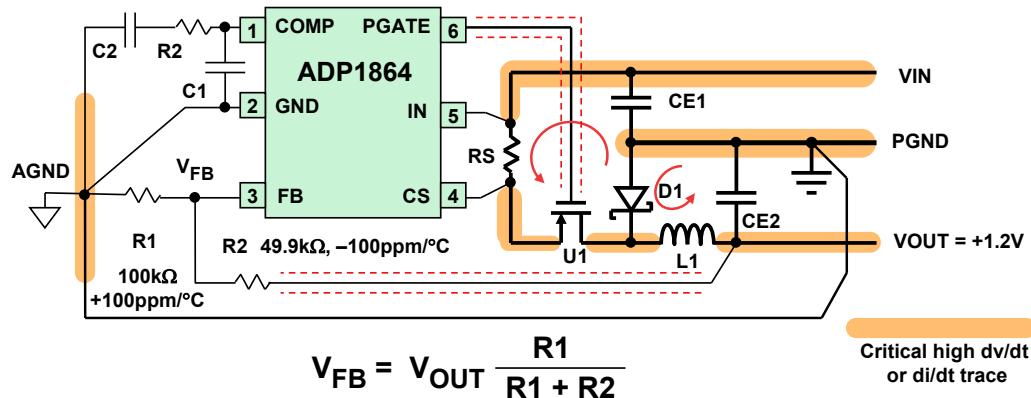
Using large area ground planes decreases the resistance, but cannot eliminate it. And from ohm's law we know that a current flowing through a resistance will cause a voltage drop across the resistance.

The resistance of a trace (or a ground plane) can be calculated by taking the resistivity of the material, which will typically be given in a resistance per unit volume (squares) of the conductor material, and multiplying by the number of the squares.

In the above example, the sheet resistance of 1 oz. copper, which is a typical PC board material, is calculated as 0.491 mΩ/square.



## Mismatched Resistor TCs Can Induce Temperature-related Gain Errors



- ◆ R1/R2 divider sets output voltage (internal reference is 0.8V)
- ◆ Assume TC of R1 is +100ppm/°C and TC of R2 is -100ppm/°C
- ◆ Temperature change of 100°C causes gain error of +0.66%
- ◆ This translates into an error of +8mV at the buck output
- ◆ Avoid further mismatch errors by keeping R1 and R2 away from heat generating components such as D1 and L1
- ◆ 1% surface mount chip resistors available in TCs to 25ppm/°C

As we have seen, processors with lower core voltages, such as FPGAs, are placing tighter tolerances on power supply voltages. The accuracy of the feedback network in this circuit must be considered as part of the overall error budget in the final output voltage. The following example illustrates the point.

For nominal resistor values  $R1 = 100\text{k}\Omega$ ,  $R2 = 49.9\text{k}\Omega$ ,  $\text{gain} = 0.6666666$

Assume that R1 and R2 have temperature coefficients of +100 ppm/°C and -100 ppm/°C, respectively.

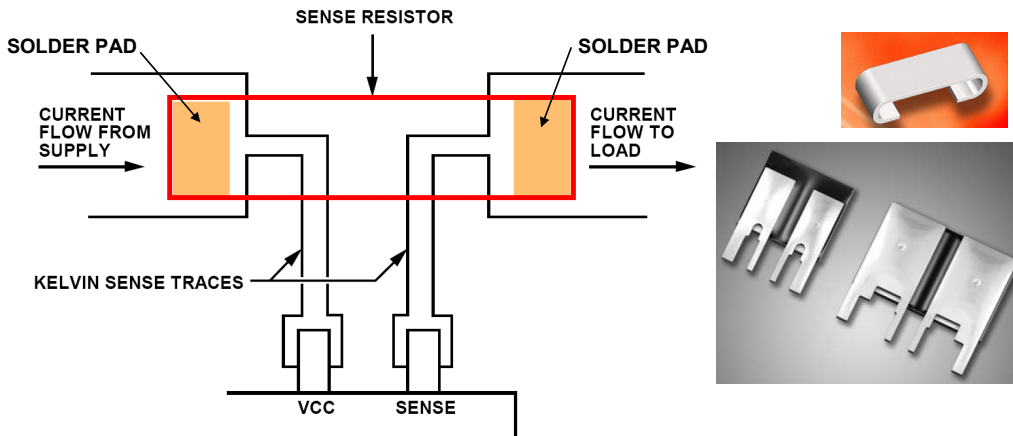
For a 100°C temperature change, R1 goes from 100 kΩ to 101 kΩ, and R2 goes from 49.9 kΩ to 49.4 kΩ. The new gain is 0.671096, which is 0.66% higher than the nominal gain. This becomes part of the overall error budget which must also include the initial resistor ratio accuracy, line/load regulation, reference accuracy, transient response, etc. Although 0.66% may seem small, the overall error budget may be less than 5% for FPGA applications.

The use of 1% surface mount chip resistors for the gain setting resistors is recommended (such as Vishay CRCW-series). TCs are available as low as 25 ppm/°C if required.

In the above diagram the red dotted line around the gate drive and feedback trace note that it should be protected from interference for external signals.

Details of layout requirements regarding switching supplies follow later in this section.

## Current Sense Resistors Require Kelvin Sensing



- ◆ If using a two pin/pad sense resistor, layout is critical to accuracy
- ◆ Kelvin sense tracks should be used at equal locations on each pad to optimize voltage drop measurement
- ◆ It is also advisable not to place the sense resistor too close to heat sources such as the MOSFET or catch diode in order to minimize temperature rise

If the current sense resistance value is low, the lead resistance may be a significant source of error. To compensate for this error it is common to use "Kelvin" (4-wire) connections, where the current flows through one pair of leads and the voltage across the resistor is sensed with a second set in which no significant current will flow. No current means no voltage drop. Such devices are, of course, more complex and so more expensive.

This figure shows how careful board layout can often make them unnecessary. The current flowing through the sense line to the  $V_{CC}$  pin is small (assuming a switching controller with external switches), and the voltage drop is usually insignificant. The load current flows through the sense resistor to the load. If the  $V_{CC}$  current is significant, then this sense trace must be made wide enough so that the voltage drop is small with respect to the drop across the sense resistor.

Medium accuracy current sense resistors often use thick film or wire-wound technology, with resistance accuracy of 1% to 5% and temperature coefficient of 20 ppm/°C to 80 ppm/°C. High precision sense resistors use metal foil resistors and can meet specifications as high as 0.1% accuracy and 5 ppm/°C temperature coefficient.

Sense resistors should not be placed close to heat sources such as MOSFET switches or catch diodes.

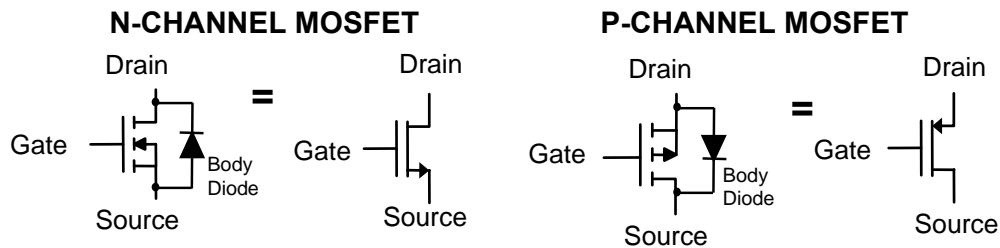
## Sense Resistor Considerations

- ◆ **Choose maximum current limit,  $I_{max}$** 
  - Select the max operating current limit. This value can be obtained from the data sheet of the controller
- ◆ **Calculate sense resistor value**
  - Using the maximum sense voltage of the controller, the sense resistor can be calculated as follows:  **$R_{sense} = V_{sense} / I_{max}$**
- ◆ **Calculate the sense resistor power**
  - The power is calculated simply as follows:  **$P = V_{sense} \times I_{max}$**
- ◆ **Determine what accuracy you will require**
  - Once all this data is determined you can choose the sense resistor. Often it is not possible to use just one resistor due to power and/or value constraints. In these case multiple resistors are used in parallel / series
- ◆ **Follow recommendations on the controller manufacturer's data sheet!!**
- ◆ **Sense resistors also used with hot swap controllers, etc.**

This figure shows some considerations regarding the selection of the sense resistor.

# Active Components

## MOSFET Basics



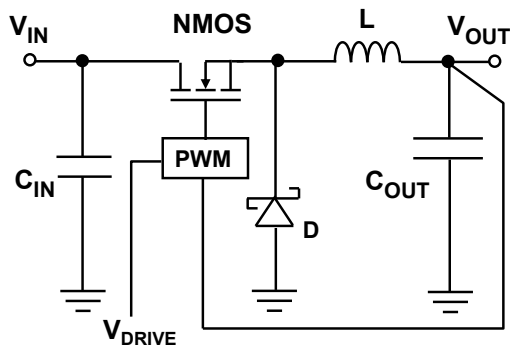
- ◆ **Three Terminal Device**
  - **Gate**
  - **Source**
  - **Drain**
- ◆ **Two classical varieties: NMOS, PMOS**
- ◆ **Electrically isolated gate**
- ◆ **High input impedance**
- ◆ **Voltage-controlled device**
- ◆ **Internal parasitic body diode from drain to source**

MOSFETs are the dominant switch technology for switch mode power supplies. Bipolar transistors are sometimes used as switches, but suffer from a number of disadvantages compared to MOSFETs.

The figure shows two common schematic representations of the NMOS and PMOS FETs. The internal parasitic body diode from drain to source is omitted in many schematics for simplification. The body diode is unavoidable due to the way MOSFETs are constructed.

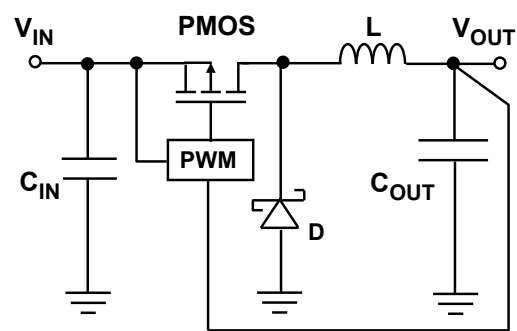
MOSFETs are easy to drive since they have high impedance inputs and are voltage-controlled devices. The only current required is to charge/discharge the parasitic gate capacitance.

## N-Channel vs. P-Channel



### N-Channel MOSFET

- ◆ More difficult to drive
- ◆ Gate must be  $V_{IN} + V_{GS(ON)}$  to turn NMOS on
- ◆ Drive voltage needed  $\geq V_{IN} + V_{GS(ON)}$
- ◆ Lower  $R_{DS(ON)}$
- ◆ Lower cost



### P-Channel MOSFET

- ◆ Easier to drive
- ◆ Gate driven below  $V_{IN}$  by at least  $V_{GS(ON)}$  to turn PMOS on
- ◆ Gate can be driven between  $V_{IN}$  and ground
- ◆ Can be run at 100% duty cycle for portable applications
- ◆ Higher  $R_{DS(ON)}$
- ◆ Higher cost

This figure summarizes the basic differences between the N-Channel and the P-Channel MOSFET. Both are shown in a typical asynchronous switching supply application.

N-Channel devices are more difficult to drive because the gate drive voltage ( $V_{DRIVE}$ ) has to be taken to a more positive voltage than the source to turn on the device. If this voltage is not available it must be generated, usually with a simple bootstrap circuit consisting of an external diode and a capacitor (the current requirement is very low). P-channel devices require drive voltages which are less than the source and therefore do not require an additional drive voltage supply. The gate of a P-Channel device can be driven between  $V_{IN}$  and ground.

P-Channel devices have intrinsically higher on resistance ( $R_{ON}$ ) due to the decreased mobility of the carriers in the P-type material. In addition, P-Channel devices are usually slightly more expensive than N-channel devices.

MOSFET current handling capability can be increased by paralleling two or more similar devices. The temperature coefficient of  $R_{ON}$  is positive which prevents current hogging. Diodes, on the other hand, have a negative TC which makes paralleling difficult.

Parallel MOSFETs reduce the effective  $R_{ON}$ , but increase the gate capacitance and the resulting switching losses.

## MOSFET Parameters of Interest for Switching Converters

- ◆ **Threshold voltage  $V_{GS(TH)}$** 
  - Minimum gate bias which enables the formation of the channel between source and drain
  - Decreases with temperature
- ◆ **On resistance  $R_{DS(ON)}$** 
  - Total resistance between source and drain during on state
  - Important parameter in determining current rating and power dissipation
  - Increases with temperature due to hole and electron mobility decreasing with temperature
  - Decreases with increased gate to source voltage
- ◆  **$R_{DS(ON)}$  has positive TC (0.7%/°C to 1%/°C)**
  - Ideal for parallel operation
  - Parallel MOSFETs tend to share current evenly
- ◆ **Drain-source breakdown voltage  $BV_{DSS}$** 
  - Maximum drain-to-source voltage device can endure without avalanche breakdown in off state.

This figure summarizes the parameters of interest when selecting MOSFETs for switching converters.

The gate threshold voltage determines the drive voltage required to turn the MOSFET on and off. It is important that this voltage does not exceed the input voltage. Otherwise, an additional supply will be needed for the drive voltage.

The on resistance determines the current rating and the power dissipation of the MOSFET. It has a positive temperature coefficient which allows multiple FETs to be paralleled without current hogging.

The drain-to-source breakdown voltage must include any transient voltage which may be generated due to the inductor switching.

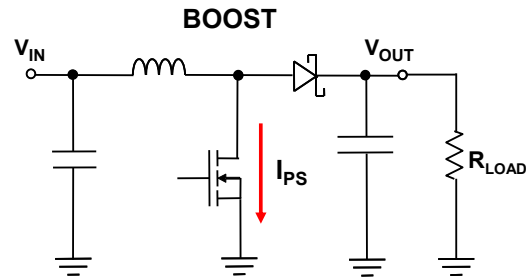
## Calculating Power in MOSFETs: Conduction Loss

- ◆ The first of two primary mechanisms of loss in a power FET is conduction loss

- ◆ Conduction loss =  $(I_{RMS})^2 \times R_{DS(ON)}$

- ◆ RMS current in Boost MOSFET

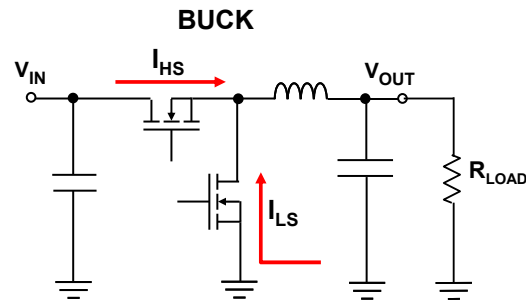
- $I_{PS(RMS)} \approx V_{IN} \sqrt{D \times 1/((1-D)^2 \times R_{LOAD})}$
- $D = t_{ON}/(t_{ON} + t_{OFF})$
- $V_{OUT}/V_{IN} = 1/(1-D)$



- ◆ RMS current in Buck MOSFET

- $I_{HS(RMS)} \approx I_{OUT} \times \sqrt{D}$
- $I_{LS(RMS)} \approx I_{OUT} \times \sqrt{(1-D)}$
- $V_{OUT}/V_{IN} = D$

- ◆ Use  $R_{DS(ON)}$  max value from data sheet at the appropriate  $V_{GS}$  drive voltage



When the FET is conducting it will be in series with an inductor for a period of the switching cycle. Knowing that inductor's dc current and ripple current values will allow you to calculate the rms current through the FET during that cycle via the following equations.

Boost (CCM) ( $\Delta I_L$  is defined as peak-to-peak inductor current) :

$$I_{PS(RMS)} = \left( \frac{V_{IN}}{(1-D)^2 \cdot R_{LOAD}} \right) \sqrt{D \left[ 1 + \left[ \frac{\Delta I_L (1-D)^2 \cdot R_{LOAD}}{2 \cdot V_{IN}} \right]^2 \frac{1}{3} \right]} \approx \frac{V_{IN} \cdot \sqrt{D}}{(1-D)^2 R_{LOAD}}$$

Buck (CCM) ( $\Delta I_L$  is defined as peak-to-peak inductor current) :

$$I_{HS(RMS)} = I_{OUT} \sqrt{D \left[ 1 + \frac{1}{3} \left( \frac{\Delta I_L}{2 \cdot I_{OUT}} \right)^2 \right]} \approx I_{OUT} \cdot \sqrt{D}$$

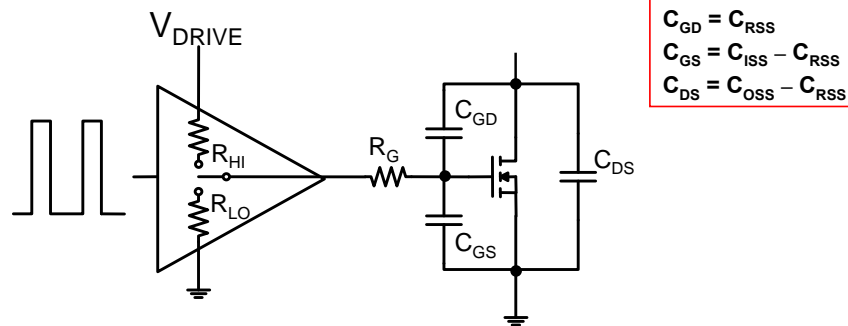
$$I_{LS(RMS)} = I_{OUT} \sqrt{(1-D) \left[ 1 + \frac{1}{3} \left( \frac{\Delta I_L}{2 \cdot I_{OUT}} \right)^2 \right]} \approx I_{OUT} \cdot \sqrt{(1-D)}$$

For a first order approximation, use the  $R_{DS(ON)}$  max value from the data sheet for the appropriate  $V_{GS}$  drive voltage. Be aware that  $R_{DS(ON)}$  increases with temperature, so calculating power dissipation due to conduction losses is actually an iterative process. However, when doing a “Will this FET work?” check, the first order approximations shown above will likely answer that question for you.



## Calculating Power in MOSFETs: Switching Loss

- ◆ The second of two primary mechanisms of loss in a power FET is switching loss
- ◆ Goal is to switch between highest resistance state and lowest resistance state as quickly as possible.
- ◆ Parasitic capacitances  $C_{GS}$  and  $C_{GD}$  slow down these transitions and thus cause power dissipation proportional to frequency.



The second source of power loss in a power FET is switching loss. Ideally, the FET switches from its highest resistance to its lowest resistance state in zero time. In practice, the finite switching time will cause switching loss.

The parasitic capacitances  $C_{GS}$  and  $C_{GD}$  slow down the transition times and cause power dissipation associated with the switching frequency.

As a reminder:

$$C_{GD} = C_{RSS}$$

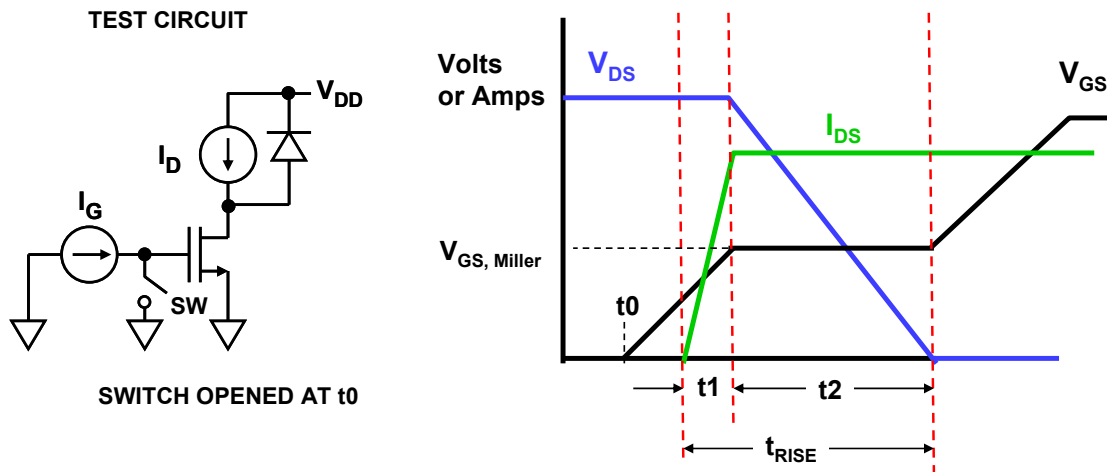
$$C_{GS} = C_{ISS} - C_{RSS}$$

$$C_{DS} = C_{OSS} - C_{RSS}$$

Note that the parasitic capacitances are voltage dependent. Therefore the values in the table of the data sheet are not very helpful. Use the capacitance versus  $V_{DS}$  curves on data sheet to determine the value of capacitance to use.

## MOSFET Switching Loss (Continued)

- ◆ The product of the current through and voltage across the inductor is a triangle wave shape. The area of this triangle is the switching transition loss.
- ◆  $P_{SW} \approx (V_{IN} \times I_{OUT}) \times F_{SW} \times (t_{RISE} + t_{FALL})/2$



This figure represents the turn on waveforms of a MOSFET.

Time period  $t_1$  is primarily due to the  $C_{GS}$  capacitance and current drive capability of the driver.

Time period  $t_2$  is the main component in slowing switching and transitions and increasing power loss.  $t_2$  is primarily due to the  $C_{GD}$  or Miller capacitance and the current drive capability of the driver.

During switching transitions (time periods  $t_1$  and  $t_2$ ) there is both voltage across drain to source and current flowing from drain to source. The presence of both current and voltage suggests there will be power dissipation in the device.

The turn off waveforms follow the same signatures. The falling waveforms would be rising and the rising waveforms falling in the turn off transition.

These losses are a function of how often the transitions occur, so switching losses increase with switching frequency.

Many other factors take this analysis beyond 1st order approximations seen here. MOSFET transconductance, reverse recovery of synchronous FETs, parasitic inductances.

$$I_{GT1} = V_{DRIVE} - 0.5 \times (V_{GS,Miller} + V_{TH}) / (R_{HI} + R_{GATE})$$

$$I_{GT2} = (V_{DRIVE} - V_{GS,Miller}) / (R_{HI} + R_{GATE})$$

$$t_1 = C_{ISS} \times (V_{GS,Miller} - V_{TH}) / I_{GT1}$$

$$t_2 = C_{RSS} \times V_{DS(OFF)} / I_{GT2}$$

$$t_{RISE} = t_1 + t_2$$

$$I_{GT3} = V_{GS,Miller} / (R_{LO} + R_{GATE})$$

$$t_{FALL} = Q_{G(SW)} / I_{GT3}$$

$$F_{SW} = \text{switching frequency}$$

## Is MOSFET Power Dissipation Too High?

- ◆ The total loss (nearly) in the FET is the sum of the switching loss and conduction loss
  - $P_{\text{TOTAL}} = P_{\text{CONDUCTION}} + P_{\text{SWITCH}}$
- ◆ Now that we have the total loss, we can determine if it is too high for thermal stability. The answer will be (as with most things) “it depends.”
- ◆ MOSFET manufacturers will specify a maximum junction temperature ( $T_{\text{JMAX}}$ ) as well as a junction to ambient thermal resistance ( $\theta_{\text{JA}}$ ) on their data sheets.
- ◆ One can roughly calculate the approximate junction temperature ( $T_{\text{J}}$ ) knowing  $\theta_{\text{JA}}$ , estimated ambient temperature ( $T_{\text{A}}$ ), and total power ( $P_{\text{TOTAL}}$ ) as follows:
  - $T_{\text{J}} = T_{\text{A}} + \theta_{\text{JA}} \times P_{\text{TOTAL}}$
  - If  $T_{\text{J}} > T_{\text{JMAX}}$ , the FET you selected will not work. (for long)
- ◆ Because MOSFET  $R_{\text{DS(ON)}}$  has a positive TC (0.7%/°C to 1%/°C), parallel MOSFETs share current fairly evenly, so parallel connections are often used in lieu of larger single FETs. Dual FETs are often connected in parallel, for example

It should be noted that  $\theta_{\text{JA}}$  is generally specified with a given type and area of copper. Chances are your design may have different copper and area. Additional analysis must be done to get a precise  $T_{\text{J}}$ . However, this 1st order approximation will likely answer the “Will this FET work?” question. There is also a linear derating factor associated with increased ambient temperature. If the design pushes the upper thermal limit, it might or might not work. Proceed with caution.

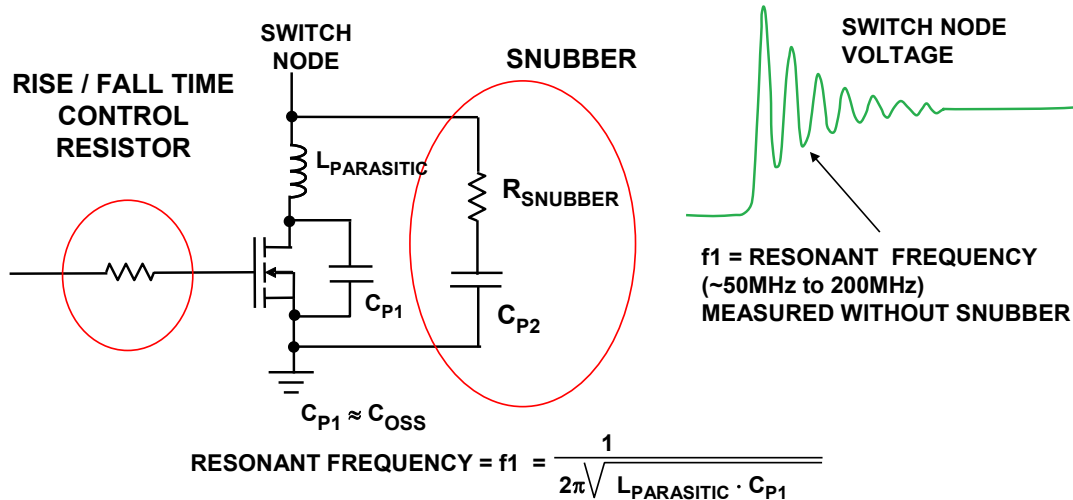
The failure mechanism in the FET is the heat itself. There is no inherent limit to the amount of current a FET can pass, so if you were running a FET with a good heat sink, the amount of power it dissipated could be significantly increased.

As indicated previously, MOSFETs can be paralleled in order to increase the total current capability at the expense of more drive current.

See the thermal design discussion later in this section.

## Snubber Selection for Buck Converters

- ◆ Not generally required for <3A applications with good layout
- ◆ Add series RC to each switching FET
- ◆ Check each switch node
- ◆ Design will have less EMI and less component stress
- ◆ Gate resistance can control rise / fall time



A *snubber* is sometimes required to protect the FET from overshoot, undershoot, and ringing at the switch node. This is caused by fast edges exciting the switch node capacitance and parasitic inductances of parts and traces. Most of the time we do not care much about this unless the spikes exceed device breakdown ratings, or the resulting EMI exceeds limits.

There is no good rule for the use of snubbers, other than use them when needed. If layout is bad, a snubber may improve EMI at most any current; but with good layout we seldom use snubbers in buck regulators under 3 A. As the current rises to >10 A snubbers are often used.

Snubbers are good at damping the ringing, but they consume power and have little effect on initial overshoot. Rise time and fall time control can be used to limit this spike—sometimes a gate resistor is used—but this method is lossy. Both methods reduce overall efficiency. A conservative approach is to initially lay out the PCB with a place for a snubber network also rise time limiting resistors, realizing that these may not be required after testing.

The figure shows an approximate equivalent circuit for designing the snubber network. When the FET current changes rapidly, ringing can occur at the resonant frequency of the FET output capacitance ( $C_{OSS}$ ) and the parasitic inductance in the loop ( $L_{PARASITIC}$ ). The frequency of this ringing is generally between 50 MHz and 200 MHz depending on circuit conditions.

Assume a resonant frequency of 100 MHz, and  $C_{OSS} = 300 \text{ pF}$ , then  $L_{PARASITIC} = 8 \text{ nH}$ .

## Snubber Selection for Buck Converters

- ◆ Apply Load to a Buck converter and measure resonant frequency (f1) on switch node transition

$$f1 = \frac{1}{2\pi \cdot \sqrt{C_{P1} \cdot L_P}}$$

- ◆ Add a reasonable amount of capacitance ( $C_{P2}$ ) whose value is somewhere between  $C_{OSS}$  of the low side FET and  $2 \times C_{OSS}$  to the switch node to ground and measure the resonant frequency again (f2).

$$f2 = \frac{1}{2\pi \cdot \sqrt{(C_{P1} + C_{P2}) \cdot L_P}}$$

- ◆ The result is two equations and two unknowns ( $C_{P1}$  and  $L_P$ )
- ◆ The next step is to find an  $R_S$  value which will slightly over-damp the LRC resonance by setting Q roughly equal to 0.9

$$Q = \sqrt{L_P / (C_{P1} + C_{P2})} / R_S$$

- ◆ The power dissipated in the snubber resistor will be  $\frac{1}{2} CV^2$  for turn on and  $\frac{1}{2} CV^2$  for turn off:

$$P = C_{P2} \cdot V_{IN}^2 \cdot f_{SWITCHING}$$

This is the first order approximation process for finding snubber values for a buck converter. Proper measurement techniques to reduce parasitics are necessary when measurement switch node resonant frequencies.

The first step is to measure the ringing frequency on the switch node, f1. Then add an external capacitor from the switch node to ground,  $C_{P2}$ , with a value between  $C_{OSS}$  (from the FET data sheet) and  $2 \cdot C_{OSS}$ . Measure the new resonant frequency, f2.

The resulting two equations can then be solved for the two unknowns,  $L_P$  and  $C_{P1}$ .

The next step is to determine the approximate value of  $R_S$  which will slightly over-damp the LRC resonance by setting Q equal to 0.9. The equation for Q can then be solved for  $R_S$ .

One can see that the added capacitance is directly proportional to the total loss in the snubber. There may be an iterative process required to find a value that minimizes losses and provides adequate damping of the ringing on the switch node.

$R_S$  and  $C_{P2}$  can be further optimized by experimentation—increase  $C_{P2}$  slightly and decrease  $R_S$ .

Snubbers are more effective the closer you can physically get them to the die voltage which you trying to snub, so the RC should be placed as close to the drain-to-source on the low side FET in a buck as possible. Make sure to adequately size the resistor to handle the power dissipation. The capacitor will not dissipate any notable amount power.

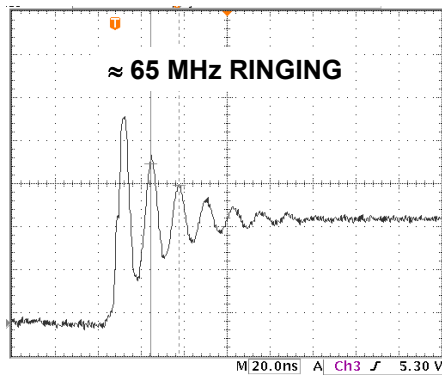
The power dissipated in the snubber resistor is approximately

$$P = C_{P2} \cdot V_{INPUT}^2 \cdot F_{SWITCHING}$$

For an example power calculation, assume  $C_{P2} = 600$  pF,  $V_{INPUT} = 12$  V,  $F_{SWITCHING} = 1$  MHz, then  $P = 86$  mW.

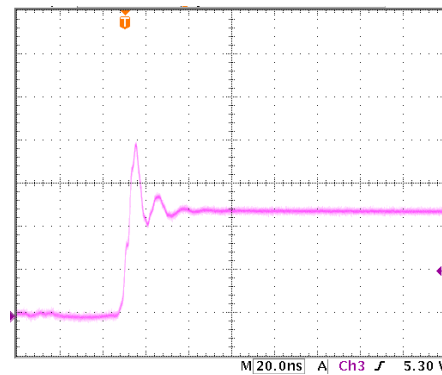
## **Effect of Snubber on the Switch Node for a Buck Converter**

**NO SNUBBER**



**VERTICAL: 5V/div  
HORIZONTAL: 20ns/div**

**WITH SNUBBER**



**VERTICAL: 5V/div  
HORIZONTAL: 20ns/div**

Here we show the effect of the snubber on the switched waveform. Note the reduction (although not elimination) of the initial overshoot and ringing.

## Diode Rectifiers

- ◆ **Standard Recovery Silicon (not recommended)**
- ◆ **Fast Recovery Silicon (not recommended)**
  - 50V to 1000V breakdown
  - 100ns to 500ns recovery time
- ◆ **"Ultrafast" Recover Silicon (only for high voltage applications)**
  - 50V to 1000V breakdown
  - 20ns to 75ns recovery time
- ◆ **Standard Schottky**
  - 20V to 100V breakdown
  - Switcher "Workhorse"
  - 0ns recovery time
- ◆ **Low Forward Voltage Schottky**
  - 10V to 40V breakdown
  - 0ns recovery time

This figure lists diode rectifiers starting with the oldest technology, standard recovery silicon diodes. These were the first type of rectifiers, such as the 1N4004 and 1N5404. Reverse breakdowns were high, but recovery time was not specified.

The addition of gold doping yielded "fast recovery" silicon diodes of 100 ns to 500 ns recovery, such as the 1N4936.

These were followed by "ultrafast" recovery silicon diodes with 20 ns to 75 ns recovery time and up to 1000 V reverse breakdown, such as the MUR140 and ES1D.

Today, the standard Schottky diode is the workhorse diode of asynchronous switchers. Certain varieties are available with breakdowns up to 200 V.

A variety of Schottky diodes are optimized for low forward voltage drop with breakdowns up to 40 V.

None of the Schottky diodes have measurable reverse recovery time.

Modern switching regulators use Schottky diodes in 99% of applications rather than the older silicon varieties.

## Diode Parallel and Series Connections



- ◆ Diodes have a negative TC, therefore one will "hog" most of the current in parallel connection. Use synchronous rectification.
- ◆ This may be useful in reducing overall parasitic inductance at the expense of additional capacitance. Cannot assume currents will share equally, however. Each diode must be rated for full current load.
- ◆ Series connection of diodes to increase effective breakdown voltage is risky and should be avoided.

The power dissipated in the diode in an asynchronous switching converter often becomes a limiting factor at high currents. Unfortunately, diodes can't be paralleled to share the current, because they have a negative forward voltage temperature coefficient.

With two diodes in parallel, one will always have a slightly lower voltage drop, and this diode will carry slightly more current than the other one, the voltage drop will decrease, it will carry even more current, and eventually it will carry all the current.

Parallel diodes can be useful in reducing the overall parasitic inductance (at the expense of increased capacitance) but will not work in current-sharing applications.

It is not advisable to connect diodes in series to increase the effective reverse breakdown.

The basic point here is that it is not advisable to try to use multiple diodes in place of one correctly sized diode in either the parallel or series connection.



# **Power Supply Layout and Grounding**

## Parasitics to Deal with in PCB Layout

- ◆ **Trace Resistance**
  - DC and AC errors due to voltage drop
  - Sheet resistance of 1 ounce copper =  $0.491\text{m}\Omega$  / square
- ◆ **Board Capacitance**
  - Coupling into high impedances and noise-sensitive circuits
  - Coupling between planes and to component pads
  - Trace capacitance =  $2.8\text{ pF/cm}^2$  for 1.5mm glass epoxy ( $\epsilon_r = 4.7$ )
- ◆ **Wiring Inductance**
  - Especially in low impedance circuits and filters
  - Use wide conductors and ground planes to minimize
- ◆ **Magnetic Coupling**
  - Inductor-to-inductor, especially toroids. Consider alternate mounting directions
  - Loop-to-loop, minimize loop areas, use ground planes

Besides the components loaded on a PC board, there are also many others parasitic elements that contribute to the performance of the circuit.

Trace resistance of the copper is approximately  $0.491\text{ m}\Omega$  / square for 1 ounce copper. For 2 ounce copper, it is one-half this value, or  $0.246\text{ m}\Omega$  / square, etc.

Trace capacitance is about  $2.8\text{ pF/cm}^2$  for 1.5 mm thick glass epoxy ( $\epsilon_r = 4.7$ ).

Trace inductance is given by the equation on p. 4.23 in this book.

Magnetic coupling between inductors, especially toroids, is also a consideration. This effect can be reduced by alternate mounting directions, minimizing loop areas, and the use of ground planes.

## Printed Circuit Board Resistance

Copper Thickness	Resistance Coefficient, milliohms/inch/w (trace width w in inches)	Reference 0.1 inch wide trace, milliohms/inch
1/2 oz/ft <sup>2</sup>	0.983/w	9.83
1 oz/ft <sup>2</sup>	0.491/w	4.91
2 oz/ft <sup>2</sup>	0.246/w	2.46
3 oz/ft <sup>2</sup>	0.163/w	1.63

**Sheet resistance of 1 ounce copper = 0.491mΩ/square**

Common values for resistance of traces for various weights of copper commonly used in PCB manufacture.

Note that not all layers of a multilayer board need to be the same weight of copper. Thinner copper can be used for signal layers, especially when using fine pitch components which require very narrow traces.

Power planes can benefit from heavier copper by lowering trace resistance and helping dissipate more heat.

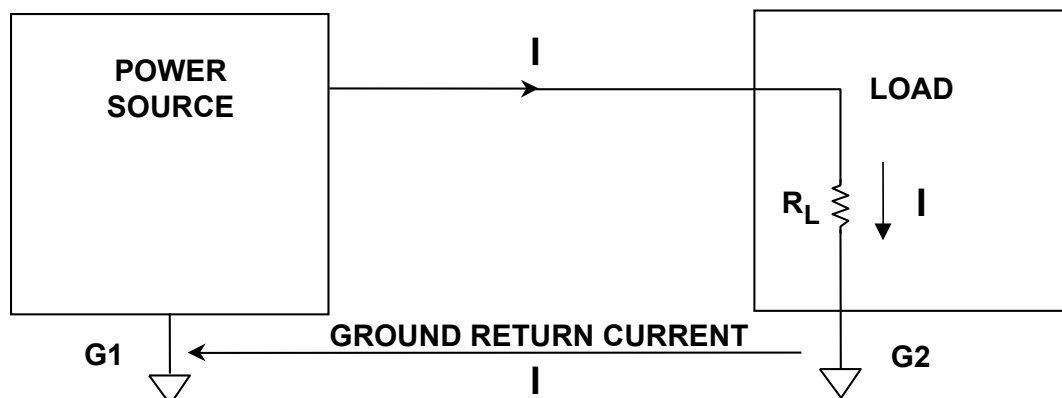
## Relative Dielectric Constant, $\epsilon_r$ , for Common PCB Materials

Laminate	Test Frequency	
	1kHz	1MHz
FR4 Glass Epoxy	4.4	4.7
FR5 Glass Epoxy	4.4	4.7
G9 Glass Melamine	7.2	7.5
G3 Glass Phenolic	5.5	
G7 Glass Silicon	4.2	4.7
Epoxy Thermount	3.9	
BT Epoxy	4.1	
Epoxy/Polymide	4.4	
Cyanide Ester	3.5	

This table shows the approximate dielectric constants of a variety of materials used in PCB dielectrics. These are rough averages of numbers from several handbooks and various manufacturers' literature, which often disagree significantly. Most are for 25°C ambient conditions, but some are measured at 20°C.

If this is an issue for your design, it is best to check with the PCB manufacturer.

## **Kirchoff's Law Helps Analyze Voltage Drops Around a Complete Circuit**



**AT ANY POINT IN A CIRCUIT  
THE ALGEBRAIC SUM OF THE CURRENTS IS ZERO  
OR  
WHAT GOES OUT MUST COME BACK  
WHICH LEADS TO THE CONCLUSION THAT  
ALL VOLTAGES ARE DIFFERENTIAL  
(EVEN IF THEY'RE GROUNDED)**

One of the biggest problems in system design is how to handle grounding. There are several competing requirements that are dependent on the frequency and system complexity.

Unfortunately, there is no magic “cookbook” approach to grounding that will always guarantee success. What we will do here is present some of the effects that must be considered when designing the system.

The main thing is to look at how and where the dc and ac currents flow in a PCB.

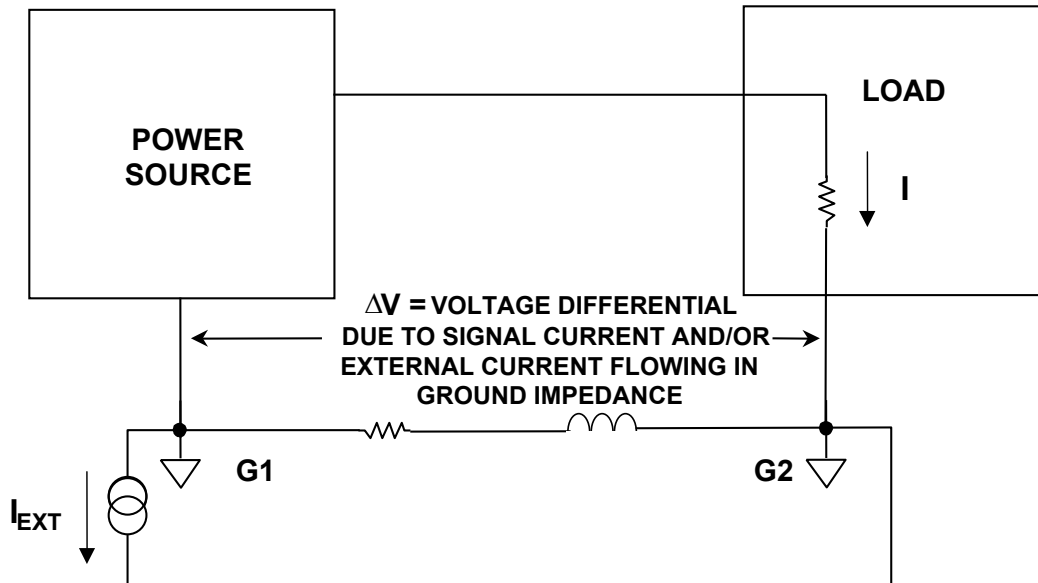
We reviewed the procedures for proper mixed-signal circuit grounding in Section 3. In this section we will look at grounding issues associated with switching power supplies.

When we draw the ground symbol on a schematic, we assume that all ground points are at the same potential. This is rarely the case, unfortunately.

Historically, “ground” was the reference level with which we measured various voltage levels in the circuit. However, ground has also become the power return not only for digital signals but for analog signals as well.

All signals that flow in a circuit must have a return path to complete the loop. Often we consider the forward path only, but there always must be a return to close the loop or current cannot flow. This return path is often through the ground plane.

## **A More Realistic View of the Impedance Between Grounds**



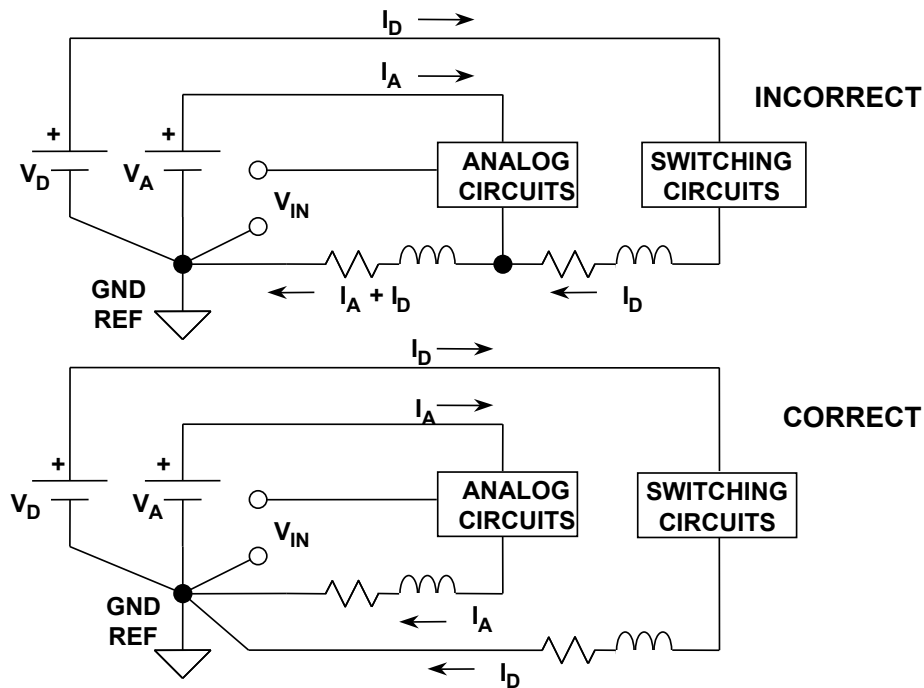
The connection between two points on the ground plane is never zero impedance. There is always some resistance and inductance, even in a large area heavy ground plane.

The magnitude of the impedance may be small, but it is not zero. And a current flowing through an impedance causes a voltage drop.

This means that the two grounds in the diagram above will not be at the same potential.

It is important to consider the inductance of the ground as well as the resistance, especially as the frequency increases.

## Switching Currents Flowing in Analog Return Path Create Error Voltages



Because ground is the power return for all digital circuits, as well as many analog circuits, one of the most basic design philosophies is to separate digital ground returns from analog ground returns.

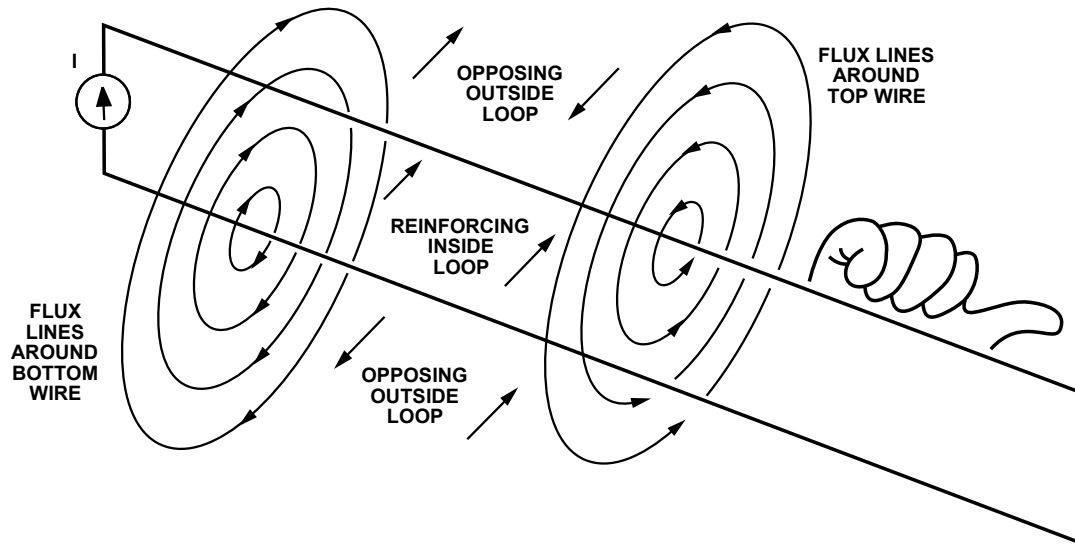
If the grounds are not separated, not only does the return from the analog circuitry flow through the analog ground impedance, but the digital ground current also flows through the analog ground, and the digital ground current is typically much greater than the analog ground current.

As the frequency of digital circuits increases, the noise generated on the ground increases dramatically. TTL and CMOS logic families are of the saturating types. This means that the logic transitions cause large transient currents on the power supply and ground. CMOS outputs basically connect the power to ground through a low impedance during the logic transitions.

And it's not just the basic clock rate that is a problem. Digital logic waveforms are basically rectangular waves, which implies many higher frequency harmonic components.

The same holds true for switching power supplies.

## Magnetic Field Lines and Inductive Loop (Right Hand Rule)

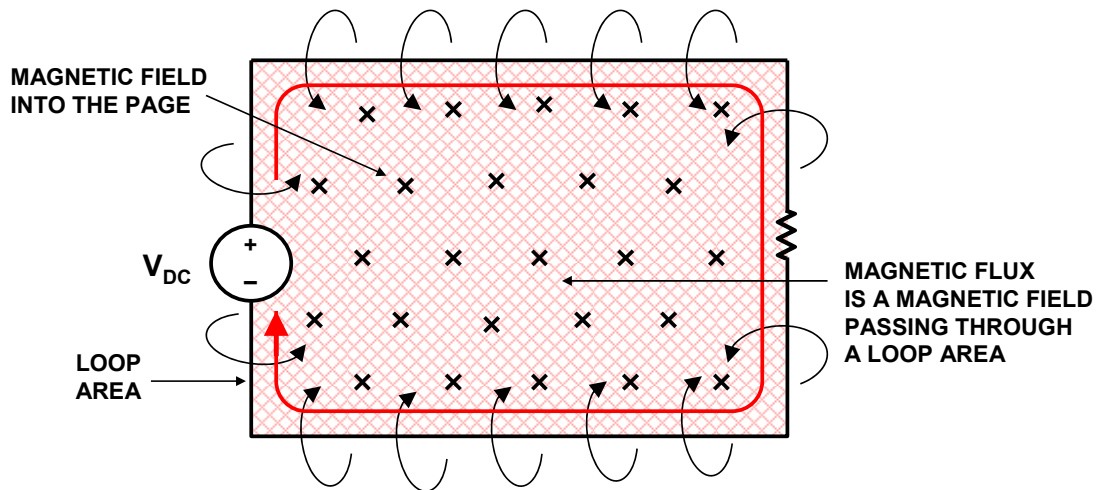


The right hand rule is useful in predicting the direction of the magnetic field lines produced by a current flowing in a conductor.

If you point the fingers of your right hand in the direction of the flux density, the induced signal will flow in the direction that your thumb is pointing.



## Magnetic Field Passing Through a Loop Area Creates Magnetic Flux



A loop of wire carrying current is essentially an electromagnet whose field strength is proportional to the current. Magnetic flux is proportional to the magnetic field passing through the loop area,

$$\text{Magnetic Flux} \propto \text{Magnetic Field} \times \text{Loop Area}$$

or more precisely,

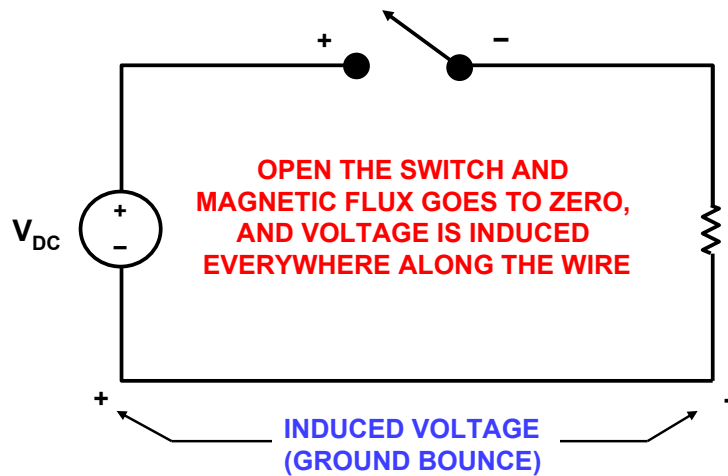
$$\Phi_B = BA \cos\phi$$

Where the magnetic flux,  $\Phi_B$ , is the magnetic field,  $B$ , passing through a surface loop area,  $A$ , at an angle,  $\phi$ , to the area's unit vector.

A look at the figure gives meaning to the magnetic flux associated with an electric current. A voltage source pushes current through a resistor and around a loop of wire. This current generates a *magnetic field* which encircles the wire. To relate the different quantities, think of grabbing the wire with your right hand (applying the *right-hand rule*). If you point your thumb in the direction of current flow, your fingers will wrap around the wire in the direction of the magnetic field lines. As those field lines pass through the loop, their product is *magnetic flux*, directed in this case into the page.

Change either the magnetic field strength or the loop area, and the magnetic flux will change. As the flux changes, a voltage is induced in the wire, proportional to the rate of change of the flux,  $d\Phi_B/dt$ . Notice that either a fixed loop and changing current or a constant current and a changing loop area—or both—will change the flux.

## Effects of Opening a Switch

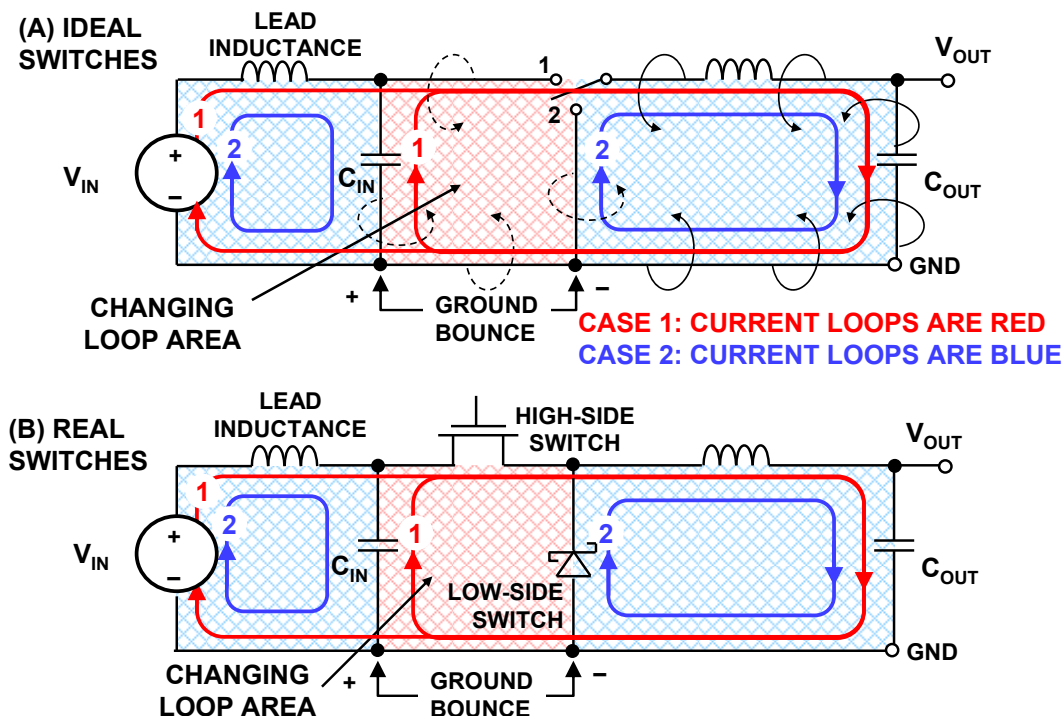


Suppose, for example, that the switch in the figure is suddenly opened. When current stops flowing, the magnetic flux collapses, which induces a momentarily large voltage everywhere along the wire.

If part of the wire is a ground return lead, voltage that is supposed to be at ground will spike, thus producing false signals in any circuitry using it as a ground reference.

Generally, voltage drops in printed-circuit-board sheet resistance are not a major source of ground bounce. 1-oz copper has a resistivity of about 500 mΩ/square, so a 1 A change in current produces a bounce of 500 mV/square—a problem only for thin, long, or daisy-chained grounds, or precision electronics.

## The Effects of Switching on Loop Area for Buck Converters



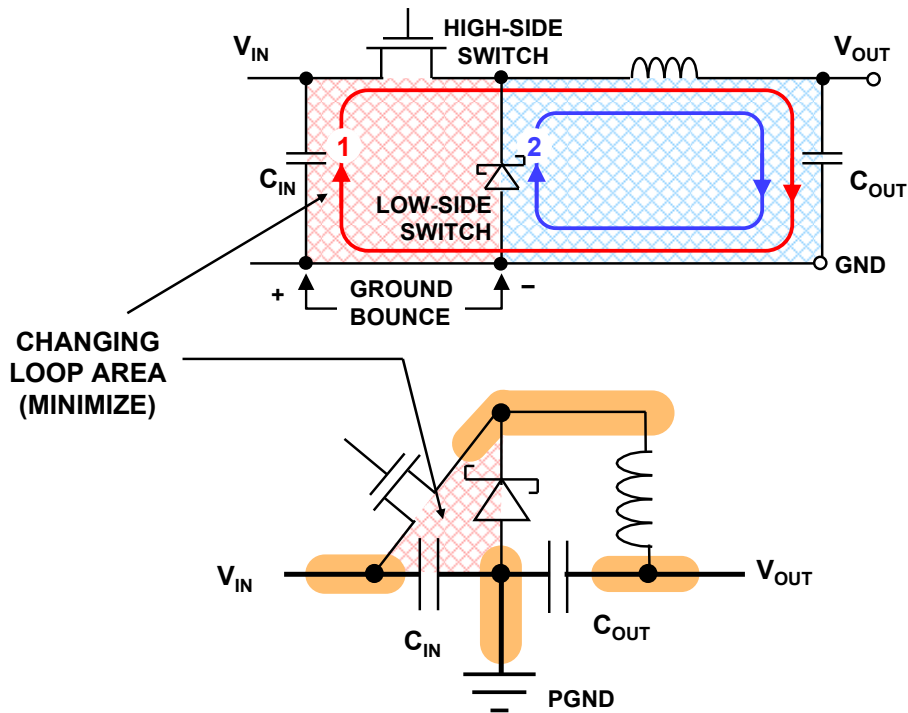
The best way to reduce ground bounce in a switching dc-to-dc converter is to control changes in magnetic flux—by minimizing both current loop *areas* and *changes* in loop area. This is illustrated in (A) which uses ideal switches. Although the input and output currents are roughly constant, as the switch moves from Position 1 to Position 2, the total loop area rapidly changes in the middle portion of the circuit. That change means a rapid change in magnetic flux, which in turn induces ground bounce along the return wire. In some cases, as in the figure, the current remains constant, but the switching produces a change of loop *area*, hence a change of flux. In (A) an ideal voltage source is connected by ideal wires to an ideal current source (the inductor represents the ideal current source). Current flows in a loop that includes a ground return. When the switch changes position, the same current flows in a different path. The current source is dc and does not change, but loop area does change. The change in loop area means a change in magnetic flux, so voltage is induced. Since a ground return is part of that changing loop, its voltage will bounce. The circuit in (B) shows the same principle implemented with real switches.

The fact that a change in magnetic flux will induce voltage everywhere along a ground return brings up the interesting question: where is true ground? Because ground bounce means a voltage on the ground return trace is bouncing with respect to some ideal point called *ground*, that point needs to be identified.

In the case of power-regulating circuits, true ground needs to be at the low end of the load. After all, a dc-to-dc converter's purpose is to deliver quality voltage and current to the load. All other points along the current return are not ground, just part of the ground return, subject to losses due to inductance and resistance.

In the following discussions, we will ignore the loop composed of  $V_{IN}$  and the lead inductance, because the current through this loop remains constant for each cycle.

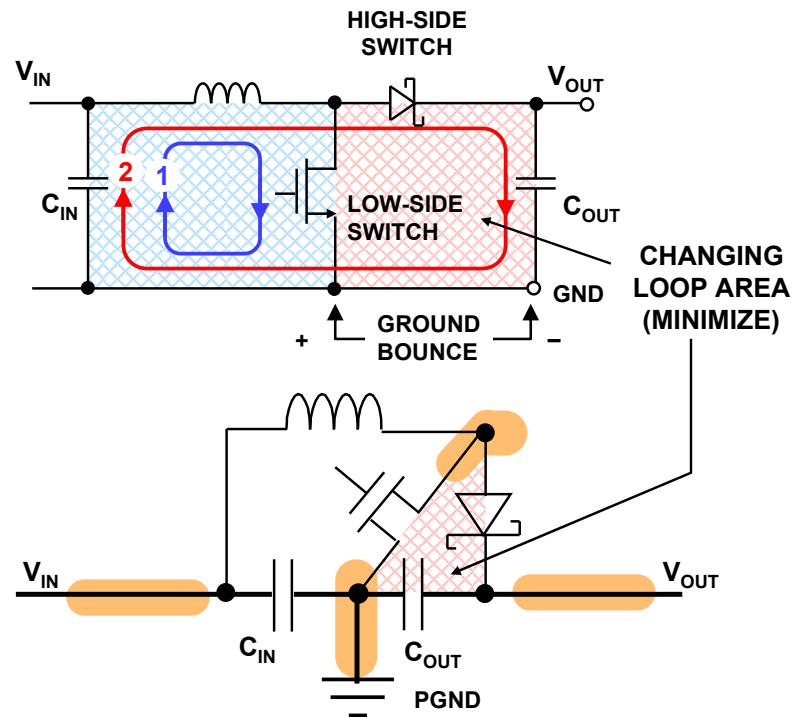
## Buck Converter Layout



This shows how the currents and loop areas change in a buck converter. A good way to minimize the ground bounce is to minimize the *changing* loop area by careful placement of the components, primarily the  $C_{IN}$  capacitor. The critical loop is comprised of the high-side switch, the diode, and  $C_{IN}$ . Capacitor  $C_{IN}$  bypasses the top of the high-side switch directly to the bottom of the low side switch, thereby shrinking the changing loop area and isolating it from the ground return. From the bottom of  $V_{IN}$  to the bottom of the load, there is only a small loop-area change from one case to the next. Consequently, the ground return bounce is minimized.

As shown in the lower diagram, both  $C_{IN}$ ,  $C_{OUT}$ , and the diode should be connected together with short leads to the power ground, designated "PGND" and shown by a triangle comprised of line segments rather than a solid triangle.

## Boost Converter Layout

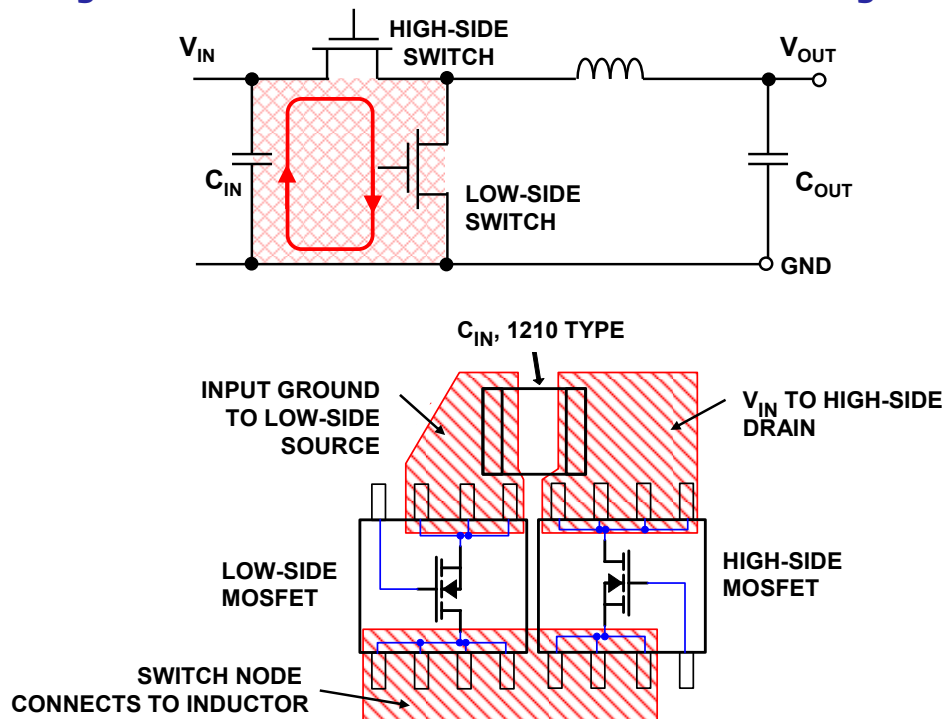


A boost converter is essentially a reflection of a buck converter, so it is the *output* capacitor that must be placed between the top of the high-side switch and the bottom of the low-side switch to minimize the change in loop area. Here the critical loop to be minimized is comprised of the low-side switch, the diode, and  $C_{OUT}$ .

Note that  $C_{IN}$ ,  $C_{OUT}$ , and the bottom of the low-side switch are connected through short leads to the PGND.

This figure and the previous one illustrate the basic principle of identifying the critical loops and minimizing their areas. This will now be applied to several actual SMPS layouts.

## Synchronous Buck Converter Layout

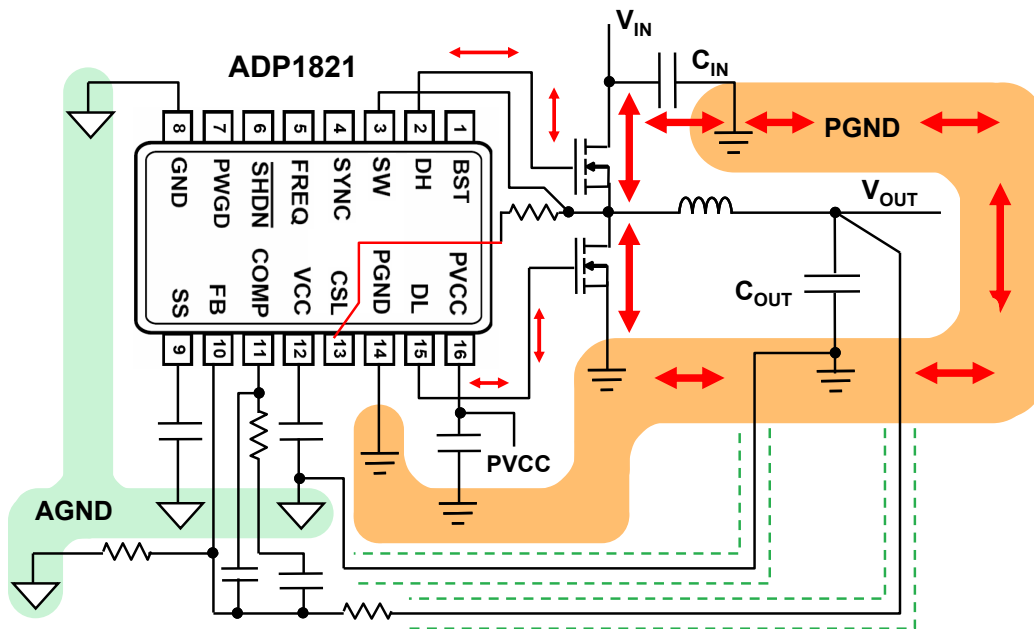


This figure shows the layout of the critical loop area in a synchronous buck converter.

Although the inductor has "continuous" high current, this current is switched alternately thru the top (control) and bottom (synchronous rectifier) FETs. The current waveform in each FET is a pulse with very high  $di/dt$ . This high  $di/dt$  flows in alternating directions in a loop comprised by the two FETs and the input bypass capacitor. Any inductance in this loop causes voltage spikes on the switch node and high-side drain with respect to the low side source, which can result in a variety of problems. To minimize this inductance, the current loop between the input bypass capacitor and thru the two FETs should be as short, fat, and tight as possible.

This example illustrates one way to get low inductance in the input ac current loop. Here, the SO-8 FETs are counter-rotated to allow shorter connections to the high current paths. The high-side drain and low-side source fit closely against the ceramic input bypass. The switch node connections fit to one compact power plane. This arrangement effectively minimizes the critical loop area composed of the switches and the input capacitor.

## ADP1821 Synchronous Buck Layout



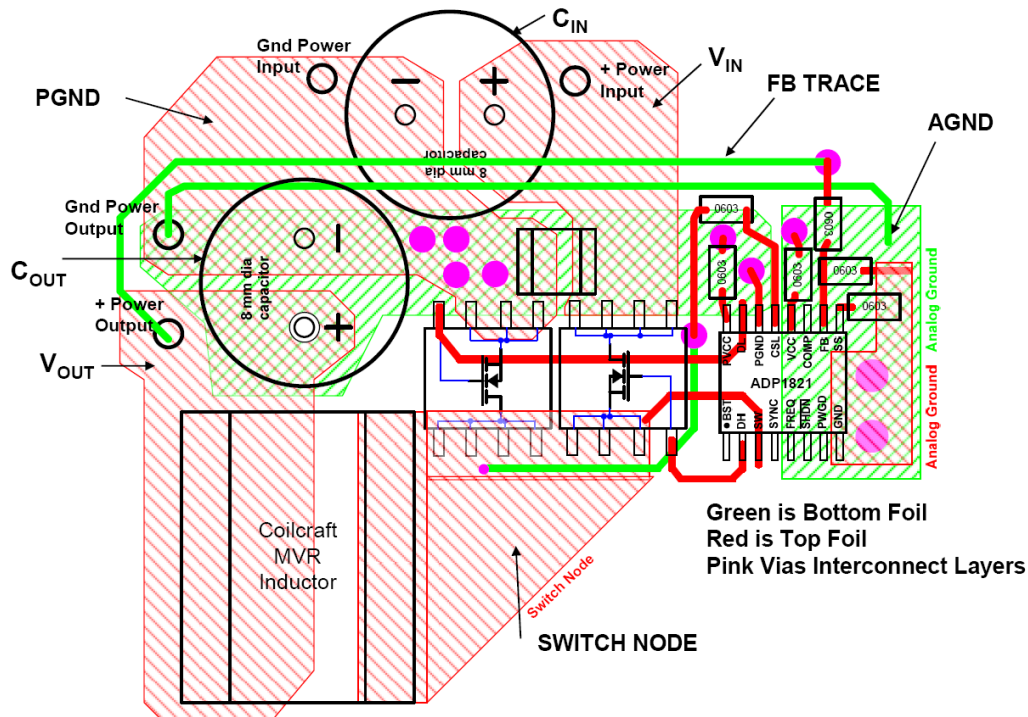
After minimizing inductance and impedance in the critical high current power paths, the second key concept is to prevent power and gate drive noise sources from interfering with the sensitive analog connections. You want to keep noise current out of traces that are noise sensitive; some of the approaches to doing this are based on Kelvin voltage sensing

ADI's design of controllers such as the ADP1821 allows significant noise voltage differential between PGND (current return path for the gate driver) and AGND (ground reference for analog circuitry). This permits a useful degree of separation of these two, which makes it easier to accomplish the desired isolation. Some competitor's ICs do not allow this separation and the layout can suffer as a result.

This figure shows schematically where the critical loop is located. All connections to the PGND island should be as short as possible. The PGND island is connected to the AGND island using a separate trace. The feedback resistors, soft-start capacitor, and the feedback compensation network should be connected to the AGND island.

Note that the output voltage is Kelvin sensed and connected to the feedback network using a separate trace. This trace should be isolated from any noisy traces.

## ADP1821 Synchronous Buck Layout Details-1



This shows details of the layout of the critical components in the ADP1821 synchronous buck layout. Note that  $C_{IN}$  and  $C_{OUT}$  are both grounded to the PGND island. The high-side and low-side FETs are rotated as previously described to minimize the critical loop area.

PGND connects directly to PGND foil. PVCC is bypassed to PGND foil with a short trace to a capacitor very close to the chip.

The AGND island is located under the ADP1821 and is connected to the PGND by a separate trace. This trace carries very little current. The FB divider,  $V_{CC}$  bypass, soft-start capacitor, and control signals are grounded to the AGND island.

This arrangement provides the most accurate ground return sense for the converter. Place components close to the IC and make connections as short as possible.

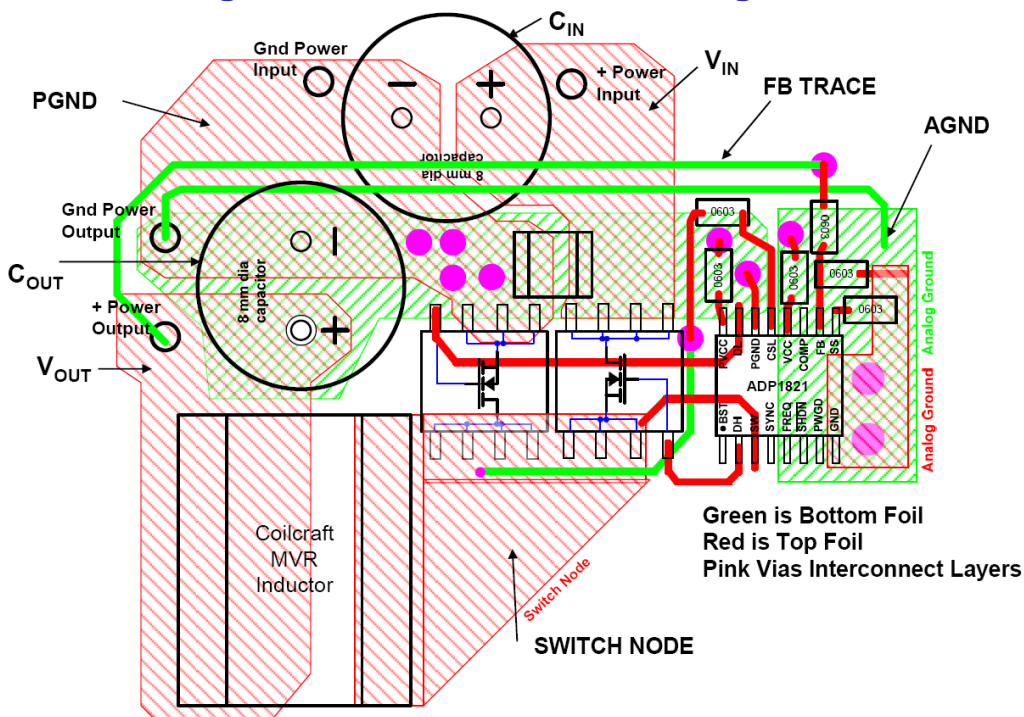
This rotation of the ADP1821 allows direct connections from the driver outputs to the FET gates. Neat, huh?

The CSL resistor connection to switch node is separate from that of SW pin for best accuracy in sensing  $V_{DS}$  on the low-side FET.

Short, fat power ground foil connects ADP1821 PGND to source leads of low side FET thru multiple vias. This provides a low impedance ground return path for gate drive current. This path is separate from analog ground.



## ADP1821 Synchronous Buck Layout Details-2

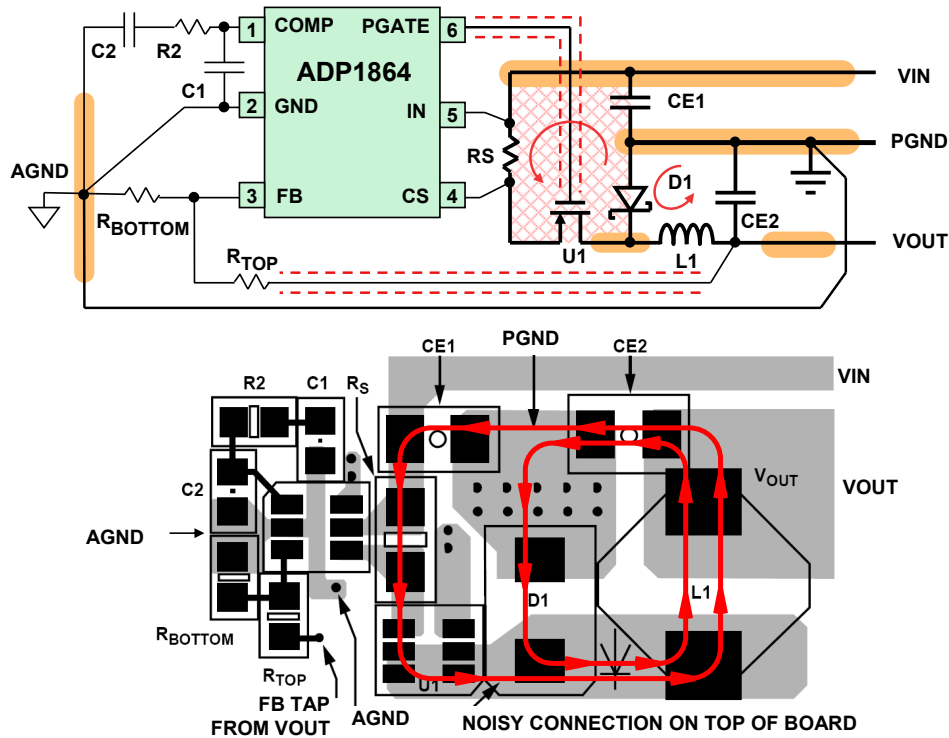


Do not run sensitive traces (such as FB, Soft Start, and Compensation) close to and parallel with noise generators such as gate drive (DH and DL) and the switch node. Parallel traces encourage inductive coupling, while mutual surface area can encourage capacitive noise coupling. Close proximity can make both worse. Where additional copper layers are available, a ground plane (placed between noise generating and noise sensitive nodes) can provide significant and helpful decoupling.

Gate drive traces (DH and DL) handle high  $di/dt$  so tend to produce noise and ringing. It is imperative that they should be as short and direct as possible. If at all possible, avoid using feedthru vias in the gate drive traces. If vias are needed, it is best to use two relatively large ones in parallel to reduce the peak current density and the current in each via.

The switch node connects the source of the high-side FET to the drain of the low-side FET and the inductor. This is the noisiest node in the switcher circuit with large ac and dc voltage and current (high  $dv/dt$  and  $di/dt$ ). This node should be wide to keep resistive voltage drop down. But to minimize the generation of capacitively coupled noise, the total area should be small. The best layout will generally place the FETs and inductor all close together on a small copper plane in order to minimize series resistance and keep the copper area small.

## Asynchronous Buck Switching Controller Layout



Here we show another example of a double-sided PCB layout for a switching supply. This is the layout of the evaluation board for the ADP1864 asynchronous buck switching controller.

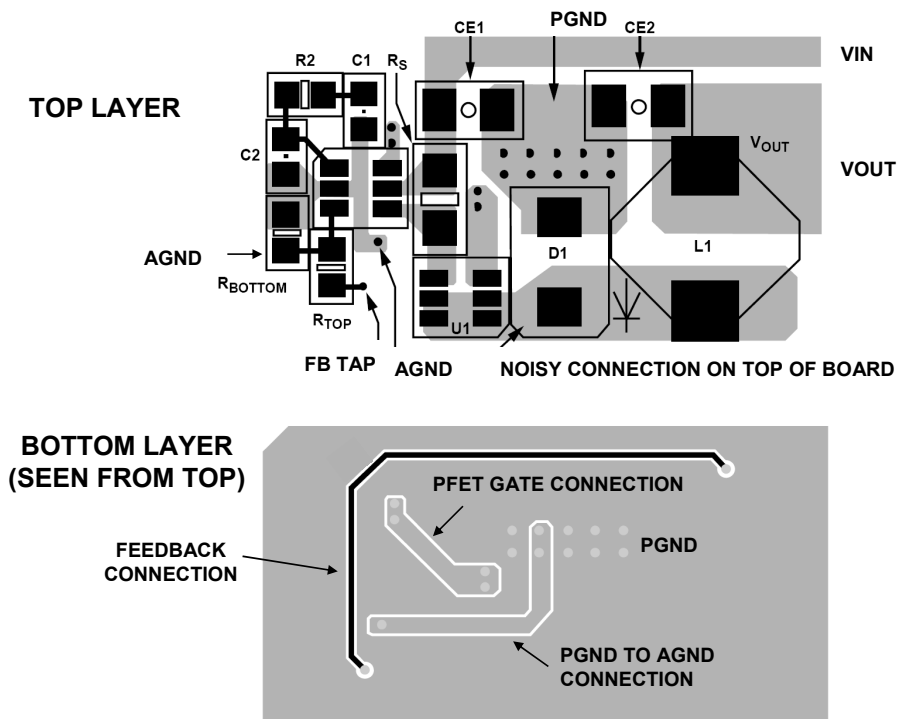
This layout follows the guidelines previously presented. The critical loop area to be minimized is comprised of the high-side FET (U1), the current sense resistor ( $R_S$ ), the input capacitor ( $CE1$ ), and the diode (D1).

Note that high  $dv/dt$  and  $di/dt$  traces and the changing loop area have been minimized.

Ground islands are used for PGND and AGND.

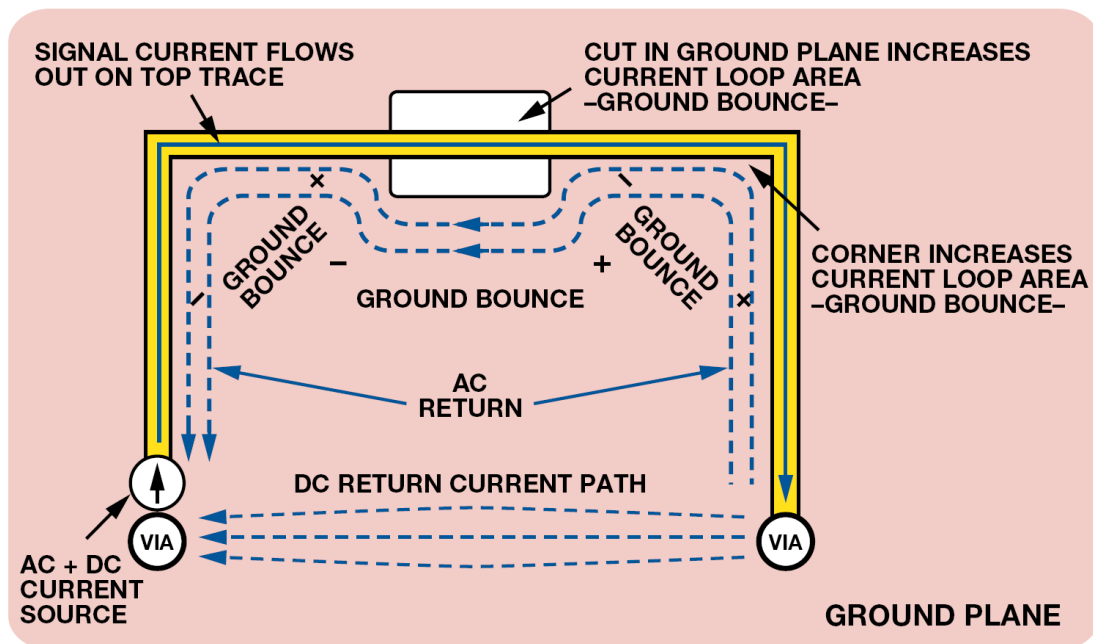
The output voltage is sensed and routed to the feedback network using a separate trace on the bottom layer of the board.

## Details of ADP1864 Double-Sided Board Layout



This figure shows the top and bottom layers of the PCB in order to see the feedback connection, and the PGND to AGND connection.

## Return Current Takes the Path of Least Impedance



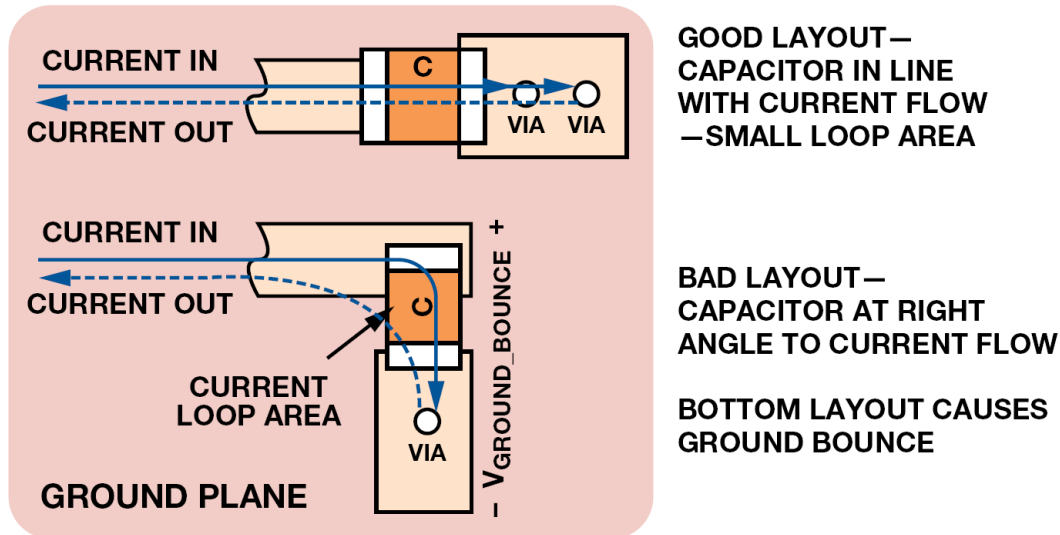
Interruptions to the ground plane under conductors carrying current can increase loop area by diverting the return current, thus increasing loop size and facilitating ground bounce. This is especially troublesome in a double-sided board.

The same thing applies for signal traces where the increased inductance and loop area can lead to increased inductive coupling of unwanted interference signals. This obviously should be avoided.

Note that the dc path is more direct than the ac path. As frequency increases the path of *least resistance* becomes the path of *least impedance*. At high frequencies return path currents tend to concentrate under the forward path (remember that all signals are really loops) to reduce inductance and therefore impedance.

Multilayer boards are almost always used in modern high-density layouts, and the ground plane breaks are much less than with simple double-sided boards.

## Effects of Component Orientation



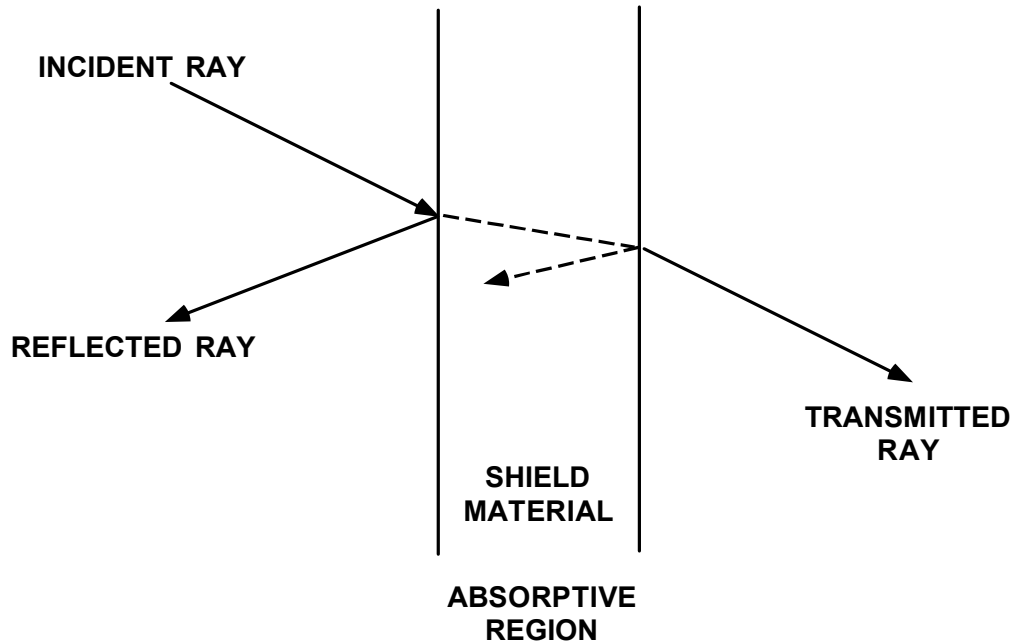
In this example, a two-layer PCB is constructed so that a bypass capacitor is attached at right angles or in-line to a top-layer supply line. In the example, the ground plane is solid and uncut. Power trace current (on the top side) flows through the capacitor, down the via, and out the ground plane.

Because ac current always takes the path of least impedance, ground return current on the lower example rounds the corner on its way back to the source. So the current's magnetic field and the associated loop area change when either magnitude or frequency of the current changes, hence the changing flux. The tendency of current to flow along the easiest path means that even a solid-sheet ground plane can have ground bounce—irrespective of its conductivity.

# Shielding

## **Reflection and Absorption Are the Two Principal Shielding Mechanisms**

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Applying the concepts of shielding requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receptor or victim). If the circuit is operating close to the source (in the near-, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the far-, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength ( $\lambda$ ) of the interference divided by  $2\pi$ , or  $\pi/2\lambda$ . If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1 ns pulse edge has an upper bandwidth of approximately 350 MHz. The wavelength of a 350 MHz signal is approximately 34 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by  $2\pi$  yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350 MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

## Conductivity and Permeability for Various Shielding Materials

MATERIAL	RELATIVE CONDUCTIVITY	RELATIVE PERMEABILITY
Copper	1	1
Aluminum	1	0.61
Steel	0.1	1,000
Mu-Metal	0.03	20,000

**Conductivity: Ability to Conduct Electricity**

**Permeability: Ability to Absorb Magnetic Energy**

For electric fields the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss. For these types of interference, high conductivity materials, such as copper or aluminum, provide adequate shielding.

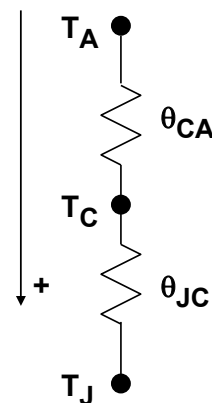
At low frequencies, both reflection and absorption loss to magnetic fields is low; thus, it is very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit.



# Thermal Design

## Thermal Design Basics

- ◆  $\theta$  = Thermal Resistance ( $^{\circ}\text{C}/\text{W}$ )
- ◆  $\Delta T = P \times \theta$
- ◆  $\theta_{JA}$  = Junction-to-Ambient Thermal Resistance
- ◆  $\theta_{JC}$  = Junction-to-Case Thermal Resistance
- ◆  $\theta_{CA}$  = Case-to-Ambient Thermal Resistance
- ◆  $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- ◆  $T_J = T_A + (P \times \theta_{JA})$ ,  $P$  = Total Device Power Dissipation
- ◆  $T_J (\text{Max})$  = Data sheet parameter. Varies device to device.



The basic concept of thermal design is to keep the junction temperature of the chip below its rated maximum junction temperature. The maximum rated junction temperature varies from device to device, but is generally between  $125^{\circ}\text{C}$  and  $150^{\circ}\text{C}$ .

The change in temperature is analogous to a resistance. The amount of power times the thermal resistance equals the temperature rise. The power is analogous to a current, and the thermal resistance is analogous to a resistance (obviously).

The thermal resistance is typically divided up into two components. The first is the thermal resistance from the junction to the case ( $\theta_{JC}$ ) and the thermal resistance from the case to the ambient ( $\theta_{CA}$ ). The  $\theta_{JC}$  is determined primarily by the package. It is typically higher for smaller packages. The  $\theta_{CA}$  can be reduced by the addition of heatsinks. The  $\theta_{JA}$  number is generally given in still air (i.e. no fans). Adding airflow will further reduce the thermal resistance somewhat.

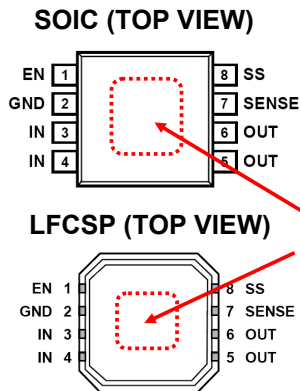
$\theta_{JA}$  is very dependent on PCB area, copper volume, and the dissipation of components around it. It is not incredibly useful because the data sheet will specify this number at one or possibly two points, which are very unlikely to be exactly like many other applications. While using  $\theta_{JC}$  to predict die temperature is not perfect, it is significantly better than using  $\theta_{JA}$ . One simply measures the temperature of the component using thermocouples or a thermal imaging device, adds that to  $\theta_{JC} \times P$  (estimated power dissipation of the IC) to find the junction temperature or  $\theta_{JC} \times P + T_C = T_J$ , where  $T_C$  is the case temperature. Note that even on a small IC, there can be “hot spots,” so it is advisable to “hunt” around that IC using thermocouples for the “hot spot.” A thermal imaging device should clearly define that spot.

ADI has an online tool to help with this calculation:

[www.analog.com/Analog\\_Root/static/techSupport/designTools/interactiveTools/powertemp/powertemp.html](http://www.analog.com/Analog_Root/static/techSupport/designTools/interactiveTools/powertemp/powertemp.html)

This tool can be accessed from the Design Center tab on the ADI website.

## ADP1706 1A LDO Power Dissipation



Exposed  
Paddle

Both packages have an exposed paddle on the bottom which should be soldered to the copper ground plane

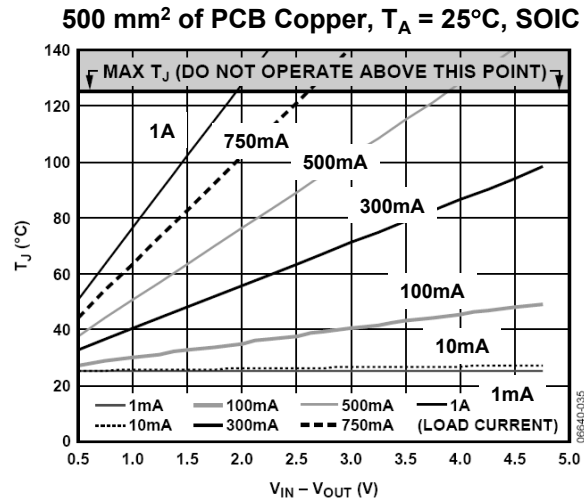


Table 5. Typical  $\theta_{JA}$  Values

Copper Size (mm <sup>2</sup> )	$\theta_{JA}$ (°C/W), SOIC	$\theta_{JA}$ (°C/W), LFCSP
0 <sup>1</sup>	57.6	65.9
50	53.1	62.3
100	52.3	61.2
300	51.3	59.7
500	51.3	59.4

<sup>1</sup> Device soldered to minimum size pin traces.

In some packages there is a lug or paddle that is meant to be soldered to the PCB. This is a means of decreasing the thermal resistance from the die to the PCB. The lug or paddle is typically the pad to which the chip is bonded and is in direct thermal contact with the die. The larger the copper land area that this lug is soldered to, the better the PCB behaves as a heatsink. Increasing copper thickness and area also increases the ability of the PCB to extract heat out of the IC.

This figure shows the thermal derating curves for the ADP1706, a 1 A LDO regulator. It is available in two packages, both of which have an exposed paddle on the bottom which should be soldered to a copper ground plane (1 ounce copper thickness). The data in the plot assumes a 500 mm<sup>2</sup> copper area and an ambient temperature of 25°C. The plot shows the junction temperature as a function of the difference between the input and output voltage for various load currents. The maximum allowable junction temperature for this device is 125°C.

A good reference for dealing with exposed paddle packages can be found at [www.analog.com](http://www.analog.com):

Gary Griffin, "A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)," Application Note AN-772, Analog Devices, 2006.

## Thermal Resistance of Popular Packages

PACKAGE	$\theta_{JA}$ (°C/W)	COMMENTS
3-lead SOT-23	300	
5-lead SOT-23	190	
6-lead SOT-23	165	
6-lead TSOT	186	ADP1864 SW Controller
8-lead SOIC	160	
16-lead QSOP	105	ADP1821 SW Controller
8-lead MSOP	75	ADP1715/ADP1716 LDOs (500mm <sup>2</sup> copper)
8-lead LFCSP (*EP)	60	ADP1706/ADP1707/ADP1708 LDOs (500mm <sup>2</sup> copper)
8-lead SOIC (*EP)	51	ADP1706/ADP1707/ADP1708 LDOs (500mm <sup>2</sup> copper)
16-lead LFCSP (*EP)	20-40	ADP2105/ADP2106/ADP2107 SW Regulators ADP1740/ADP1741 LDOs
SOT-223	65	ADP3338/ADP3339 LDOs (1 in <sup>2</sup> copper), $\theta_{JC} = 27^{\circ}\text{C/W}$
TO-220	35	(1 in <sup>2</sup> copper), $\theta_{JC} = 3^{\circ}\text{C/W}$
TO-263 (D2PAK)	35	(1 in <sup>2</sup> copper), $\theta_{JC} = 3^{\circ}\text{C/W}$

\*EP = Exposed Paddle

Above values are typical, consult product data sheet for exact value

Here are some example  $\theta_{JA}$  numbers for some popular IC packages, especially those commonly used for power circuits.

It should be noted that there can be some variation in these numbers between different manufacturers depending upon the method of measurement, PCB mounting, etc.

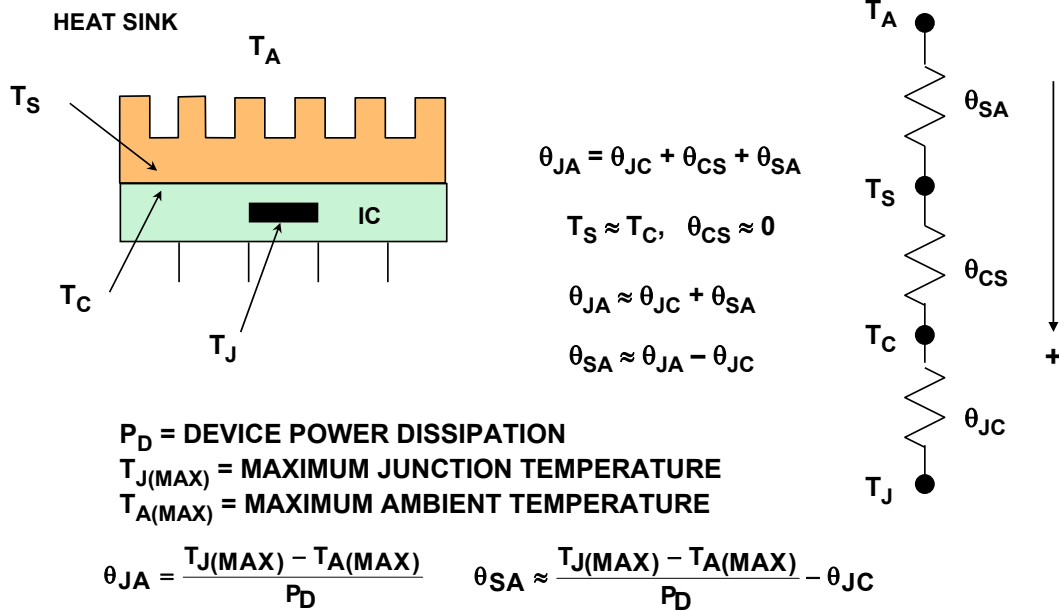
See also:

[www.analog.com/Analog\\_Root/static/Packages/ThermalDataWP.pdf](http://www.analog.com/Analog_Root/static/Packages/ThermalDataWP.pdf)

This can also be accessed from the Package Thermal Characteristics tab on the heat sink design tool.

[www.analog.com/Analog\\_Root/static/techSupport/designTools/interactiveTools/powertemp/powertemp.html](http://www.analog.com/Analog_Root/static/techSupport/designTools/interactiveTools/powertemp/powertemp.html)

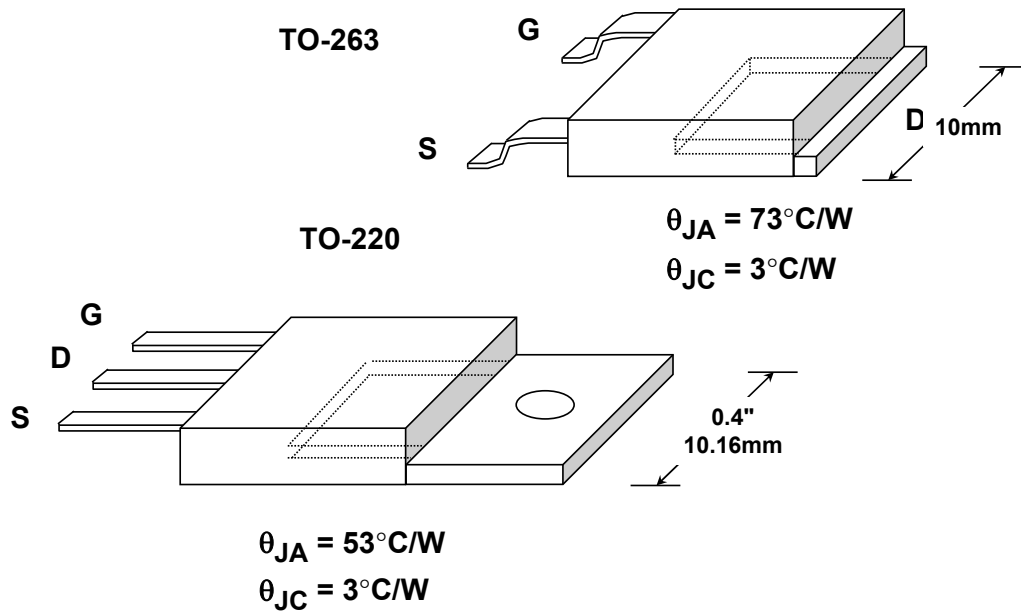
## Heat Sink Basics



The fundamental purpose of heat sinks and airflow is to allow high power dissipation levels while maintaining safe junction temperatures. There are many tradeoffs which can be made between airflow and heat sink area, and this section examines some of them.

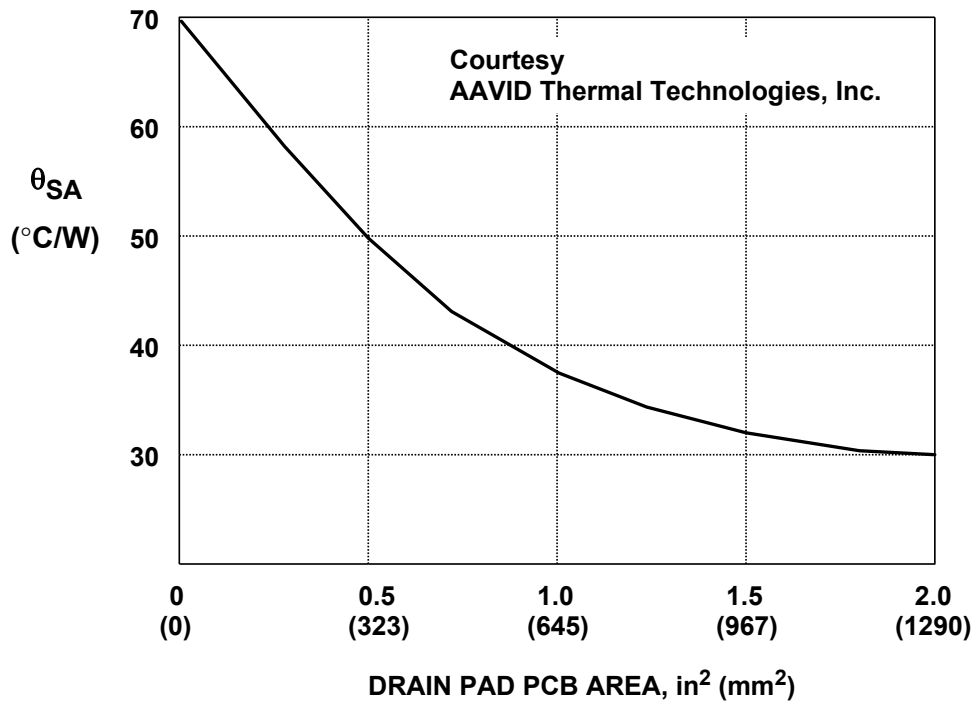
A thermal model of an IC and a heat sink is shown in this figure. The critical parameter is the junction temperature,  $T_J$ , which must be kept below 150°C for most ICs. The model shows the various thermal resistances and temperatures at various parts of the system.  $T_A$  is the ambient temperature,  $T_S$  is the heat sink temperature,  $T_C$  is the IC case temperature, and  $T_J$  is the junction temperature. The heat sink is usually attached to the IC in such a manner as to minimize the difference between the IC case temperature and the heat sink temperature. This is accomplished by a variety of means, including thermal grease, machined surface contact area, etc. In any case, the thermal resistance between the heat sink and the IC case can usually be made less than 1°C/W to 5°C/W.

## **TO-220 and TO-263 (D<sup>2</sup>PAK) Packages**



This figure shows two standard packages which are capable of dissipating considerable power. Also note that the drain (D) connection for the TO-263 package is electrically connected to the slug. This means that electric isolation from the heatsink is required for safety.

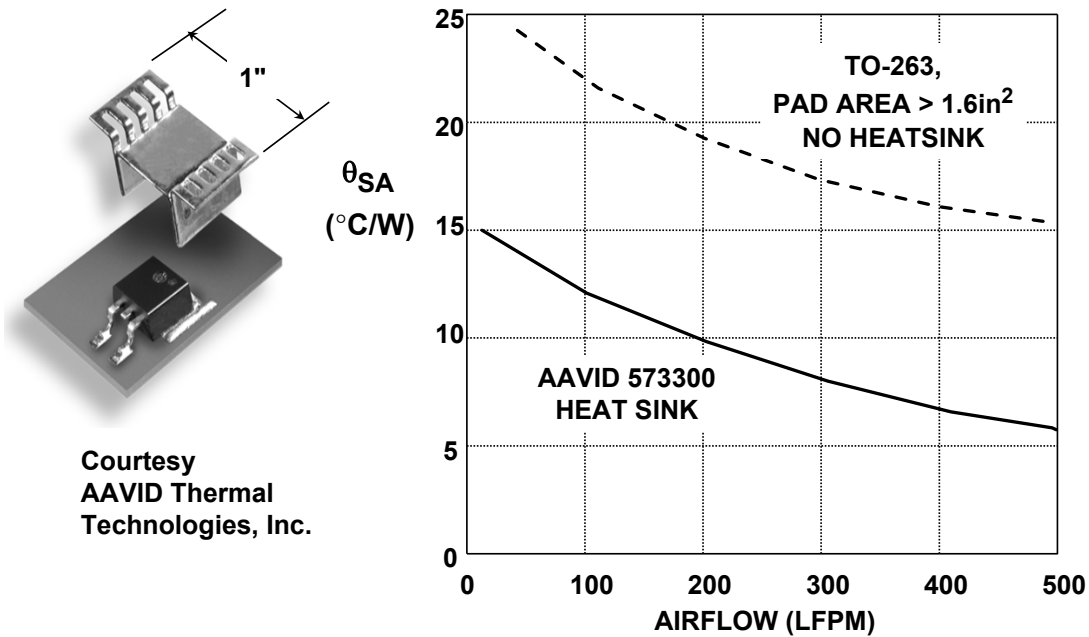
## **Thermal Resistance of TO-263 (D<sup>2</sup>PAK) vs. Drain Pad Area—No Airflow**



The thermal resistance of a TO-263 package soldered to a PCB land area. Obviously, a larger PCB land area will make a better heatsink. Copper is a fairly effective conductor of heat (as well as electricity). Again, this is in still air. Airflow will help some (see next page).

This figure shows the thermal resistance of the TO-263 package as a function of PC board drain pad area which is acting as the heat sink. Note that even with 2 square inches of pad area, the thermal resistance is still 30°C/W.

## Thermal Resistance of AAVID 573300 Surface Mount Heat Sink vs. Airflow



The situation can be improved by the addition of a surface-mount heat sink as shown in this figure (AAVID part number 573300). This heat sink solders to two pads on the PC board which are extensions of the drain pad connecting area. The thermal resistance of this combination as a function of airflow is shown in this figure.

Note that with the addition of the surface-mount heat sink, the thermal resistance of the combination is reduced to approximately 10°C/W with a reasonable amount of airflow (200 linear feet per minute). The curve also shows the thermal resistance with no heat sink as a function of airflow, clearly indicating that a heat sink definitely is effective for high power dissipation.



## Technical References

## Analog Devices' Textbook References

1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. See Chapter 12.
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## Notes: